3 Semiconductor Diodes

3.1 Introduction

When one half of a single piece of semiconductor crystal is doped with *P*-type impurities and other half by *N*-type impurity, then a plane dividing these zones is called a *P-N* junction as shown in Fig. 3.1. In this figure, ⊖ symbol means acceptor ions, ○ means hole, ⊕ means donor ion and ● means electron.

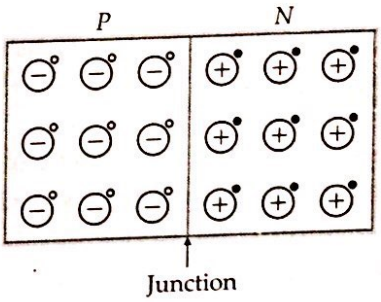


Figure 3.1 *P-N* junction

When a *PN* junction is packed as a semiconductor device, it is called *PN junction diode*.

It may be noted that a useful *P-N* junction cannot be produced by connecting *P*-type material to a *N*-type material by welding, sholdering etc. because it causes discontinuity of lattice structure at the junction. The common procedure to develop a *PN* junction is adding acceptor impurity (*P*-type) on one side and donor impurity (*N*-type) on the other side of the same crystal, so that there is no discontinuity of lattice at the junction.

Such a *PN* junction may be produced by any of the following methods :

(*i*) Grown Junction
(*ii*) Fused or Alloy Junction
(*iii*) Diffused Junction
(*iv*) Recrystallised Junction
(*v*) Point Contact Junction
(*vi*) Surface Barrier Junction

Out of these the *first three* methods are usually used :

(*i*) Grown Junction

In this method, a single crystal seed of a tetravalent semiconductor (*e.g.*, germanium) is touched with the liquid surface of molten germanium and is slowly withdrawn when the seed is withdrawn, the molten germanium crystallises into the seed in the form of the additional lattice layers and the crystal grows. Now an acceptor impurity (*e.g.*, indium) is added to melt so that a *P*-type crystal is obtained. When the *P*-type crystal has attained the sufficient size, a donor impurity (*e.g.*, arsenic, phosphorous) is added to melt in a quantity sufficient to have the effect of donor type impurity, so the remainder portion of the crystal is *N*-type. The grown junction is shown in Fig. 3.2.

Figure 3.2 Grown junction

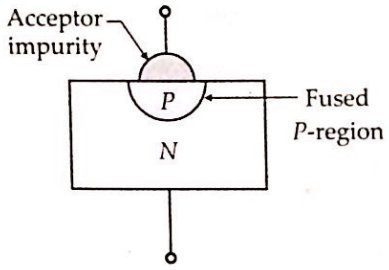


Figure 3.3 Fused junction

(*ii*) Fused or Alloy Junction

A small 'pellet' of acceptor impurity (*e.g.*, indium) is pressed on a wafer of *N*-type semiconductor. The combination is then heated about 1250° C in order to melt the impurity which diffuses a short distance into the wafer thereby producing a *P*-type region. A *P*-*N* junction is thus formed between the *P*-region and the remainder of *N*-type semiconductor as shown in Fig. 3.3.

(*iii*) Diffused Junction

In this process, a slab of *N*-type material is exposed to a gaseous impurity of *P*-type. The slab is heated to high temperature. The gaseous impurity diffuses slowly into the surface of semiconductor. The concentration of impurity is maximum at the surface and decreases rapidly inward. Thus a *PN* junction is formed directly under the surface. The diffusion junction is shown in Fig. 3.4.

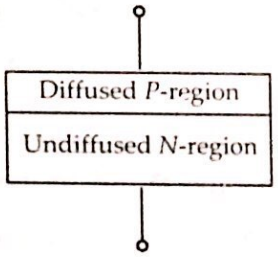


Figure 3.4 Diffused junction

During the formation of *PN*-junction, following *three* phenomena take place :

(*i*) A thin *depletion layer* (thickness $\cong 10^{-6}$ m) is formed on both sides of the junction and is so called because it is free of mobile charge carriers.

(*ii*) A *potential barrier* is developed across junction.

(*iii*) The presence of depletion layer gives rise to junction and diffusion capacitance.

3.2 Theory of *P-N* Junction Diode

The contact surface obtained by suitably joining a *P*-type semiconductor with *N*-type semiconductor and separated by a thin junction is called *PN*-junction diode or junction diode.

The circuit symbol for a normal diode is shown in Fig. 3.5.

Figure 3.5 Circuit symbol of a normal semiconductor diode.

3.2.1 *PN*-junction Diode with No Applied Voltage

The *PN*-junction diode is shown in Fig. 3.6. In this diode, the *N*-type semiconductor is at the right and *P*-type is at the left. The *P*-region has holes (white) and the *N*-region electrons (black) available as majority carriers. Note that a few electrons are also present in *P*-region, and a few holes in the *N*-region, which are minority carriers and make no substantial contribution to any conduction.

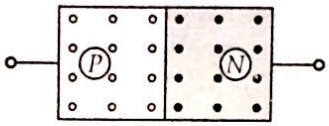


Figure 3.6 *PN* junction before diffusion.

Formation of Depletion Layer

From Fig. 3.6, it seems at first glance that even when no external connections are made to crystal, the excess electrons in the *N*-region would immediately cross the junction and combine with the excess holes in the *P*-region. This action actually starts to occur, but before it can progress very far, it is brought to halt. This is because the moment of some of electrons in the *N*-regions cross the junction and combine with the corresponding number of holes in the *P*-region, the electrical neutrality of the two regions is upset. The *N*-region loses electrons, causing it to become positively charged, while the *P*-region loses its positive holes through combination with the electrons from the *N*-region, causing it to become negatively charged. The positive and negative charges in *N*- and *P*-regions respectively increase as the number of departed electrons increase, and a point is quickly reached at which this migratory action is halted. An additional electron from the *N*-section attempting to cross the junction is not only attracted by the net positive charge of its own section, but is also repelled by the net negative charge of the *P*-section. In the similar manner the holes in *P*-region are preventing from crossing the junction by the attractive force due to the net negative charge of its own section and also by the repulsive force due to the net positive charge of the *N*-section. The net effect of the diffusion of charge carriers across the junction is the creation on each side of the junction of a thin layer that is depleted (emptied) of mobile charge carrier (*i.e.*, free electrons and holes) as shown in Fig. 3.7.

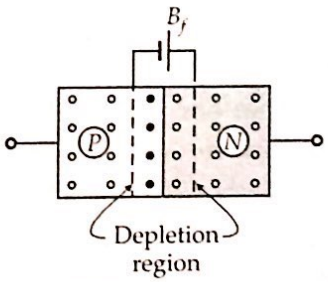


Figure 3.7 Depletion region of a *PN*-junction.

This is known as the *depletion layer*, the *space-charge region*, the *transition region* or simply *the junction region*. The thickness of the depletion layer is usually of the order of 10^{-6} m (1 μm). This depletion region is similar to the dielectric in a charged capacitor.

Barrier Potential

The opposition to the movement of electrons and holes from crossing the junction is called a *potential hill*. The electrons in *N*-region have to climb a negative potential hill as shown in Fig. 3.8, in order to reach the *P*-region. The hill of course, is the repelling force of the acceptor atoms. Similarly, the holes in *P*-region have to climb a positive potential hill, which represents the restraining forces present at the junction, can also be represented by a fictitious battery B_f connected across the junction as shown in Fig. 3.8. The negative terminal of the battery is connected to the *P*-region, while the positive terminal is connected in the *N*-region. Electrons are trying to cross from the *N*-region to *P*-region experience a retarding field of the battery and are therefore, repelled. Similarly, the holes trying to cross from the *P*-region to *N*-region are repelled. Potential thus produced is called the *potential barrier* and is of the order of 0.3 V for Ge and 0.7 V for Si. Indeed only a few majority carriers with sufficient energy succeed in crossing.

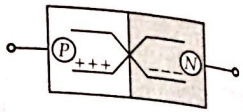


Figure 3.8 *PN* junction : potential hill.

Energy Level Diagram

An energy level diagram for the *P-N* junction is shown in Fig. 3.9. Because the *P*-region has lost some high energy holes, and gained some high energy electrons and therefore, is no longer electrically neutral, its energy level diagram will be relatively displaced above that of the *N*-region by an amount of energy equal to eV_0, where e is the charge on the electron and V_0 is the electrostatic potential difference across the junction.

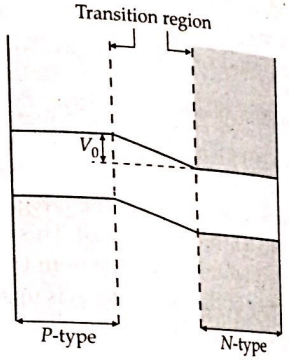


Figure 3.9 *PN* junction : Energy level diagram

Expressions for Width of Depletion Layer and Potential Barrier

As soon as the *PN*-junction is formed, the diffusion of holes (from *P*-region to *N*-region) and electrons (from *N*-region to *P*-region) takes place for a short time and then force (called a barrier) is automatically developed across the junction which stops the further diffusion of holes and electrons from one side to the other. The difference of potential from one side of the barrier to the other side is called the *height of the barrier*.

Figure 3.10 shows the variation of potential with distance along the junction. It is shown that barrier potential is given by

$$V_B = V_N + V_P \qquad ...(3.1)$$

where V_N and V_P are the magnitudes of the potential rise and fall in *N* and *P* regions.

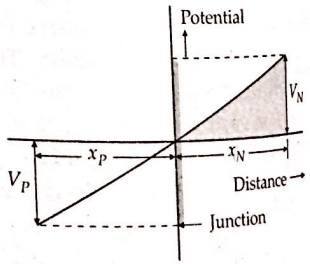


Figure 3.10 Potential vs. distance.

The width of the depletion region is given by

$$x = x_N + x_P \qquad ...(3.2)$$

where x_N and x_P are the width of depletion layer in *N*-and *P*-regions respectively.

To find the distribution of barrier potential, we start with Poisson's equation in one dimensional which is

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon} \qquad ...(3.3)$$

where ρ is the volume density of charge and ε is the permittivity of the medium.

The charge density in *P*-side of depletion layer is given by

$$\rho = -eN_A \qquad ...(3.4)$$

where N_A is the density of completely ionized acceptor atoms. Therefore, Eq. (3.3) for *P*-side of depletion layer becomes

$$\frac{d^2V}{dx^2} = \frac{eN_A}{\varepsilon}$$

Integrating it, we have

$$\frac{dV}{dx} = \frac{eN_A x}{\varepsilon} + A \qquad ...(3.5)$$

where *A* is the constant of integration.

Applying boundary condition : when $x = -x_p$, $\frac{dV}{dx} = 0$, we get

$$A = \frac{eN_A}{\varepsilon} x_p$$

Putting this value in Eq. (3.5), then we have

$$\frac{dV}{dx} = \frac{eN_A}{\varepsilon} x + \frac{eN_A}{\varepsilon} x_p = \frac{eN_A}{\varepsilon} [x + x_p]$$

Integrating the above equation, we get

$$V = \frac{eN_A}{\varepsilon} \left[\frac{x^2}{2} + x_p x \right] + A' \qquad ...(3.6)$$

A' being a new constant of integration.

But at junction, where $x = 0$, $V = 0$

$\therefore \qquad A' = 0$

Then, Eq. (3.6) is termed as

$$V = \frac{eN_A}{\varepsilon} \left[\frac{x^2}{2} + x_p x \right] \qquad ...(3.7)$$

Also when $x = -x_P$, $V = V_P$, then

$$V_P = \frac{eN_A}{\varepsilon}\left[\frac{x_P^2}{2} - x_P^2\right] = -\frac{eN_A x_P^2}{2\varepsilon}$$

or
$$|V_P| = \frac{eN_A}{2\varepsilon} x_P^2 \qquad \text{...(3.8)}$$

Similarly, the Poisson's equation, for N-size of depletion layer is

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon} = -\frac{eN_D}{\varepsilon} \qquad \text{...(3.9)}$$

where N_D is the density of completely ionised donor atoms.

Proceeding as above and applying boundary conditions : where $x = 0, V = 0$ and when $x = x_N$, $\frac{dV}{dx} = 0$ and $V = V_N$, then we get

$$|V_N| = \frac{eN_D}{2\varepsilon} x_N^2 \qquad \text{...(3.10)}$$

Therefore, the height of potential barrier across the junction

$$V_B = |V_N| + |V_P|$$

$$= \frac{eN_D}{2\varepsilon} x_N^2 + \frac{eN_A}{2\varepsilon} x_P^2 = \frac{e}{2\varepsilon}[N_D x_N^2 + N_A x_P^2] \qquad \text{...(3.11)}$$

Since in thermal equilibrium, the electric field far from the junction at either side of the semiconductor must be zero, the negative charge per unit area in the P-side must be exactly equal to the total positive charge per unit area in the N-side.

Therefore

$$N_A x_P = N_D x_N \qquad \text{...(3.12)}$$

Putting the value $x_N = \frac{N_A}{N_D} x_P$ in Eq. (3.11), we get

$$V_B = \frac{eN_A}{2\varepsilon}\left[1 + \frac{N_A}{N_D}\right] x_P^2 \qquad \text{...(3.13)}$$

It gives
$$x_P = \left[\frac{2\varepsilon V_B}{eN_A[1 + N_A/N_D]}\right]^{1/2} = \left[\frac{2\varepsilon V_B}{e}\frac{N_D/N_A}{(N_A + N_D)}\right]^{1/2} \qquad \text{...(3.14)}$$

Similarly, we can obtain

$$x_N = \left[\frac{2\varepsilon V_B}{eN_D[1 + N_D/N_A]}\right]^{1/2} = \left[\frac{2\varepsilon V_B}{e}\left(\frac{N_A/N_D}{N_A + N_D}\right)\right]^{1/2} \qquad \text{...(3.15)}$$

Therefore total width of depletion layer

$$x = x_N + x_P = \left[\frac{2\varepsilon V_B}{e(N_A + N_D)}\right]^{1/2} \times \left[\left(\frac{N_A}{N_D}\right)^{1/2} + \left(\frac{N_D}{N_A}\right)^{1/2}\right] \quad ...(3.16)$$

If $N_D > N_A$, then $(N_A + N_D) \to N_D$ and $\frac{N_A}{N_D} \to 0$

Then Eq. (3.16) becomes

$$x = \left(\frac{2eV_B}{eN_D}\right)^{1/2} \times \left(\frac{N_D}{N_A}\right)^{1/2} = \left(\frac{2\varepsilon V_B}{eN_A}\right)^{1/2} \quad ...(3.17)$$

Equation (3.17) shows that the width of depletion layer decreases with increase in impurity concentration. Further from Eqs. (3.8) and (3.10), we get

$$\frac{V_P}{V_N} = \left(\frac{x_P}{x_N}\right)^2 \left(\frac{N_A}{N_D}\right) \quad ...(3.18)$$

Also from Eqs. (3.14) and (3.15), we get

$$\frac{x_P}{x_N} = \frac{N_D}{N_A} \quad ...(3.19)$$

Substituting Eqs. (3.19) in Eq. (3.18), we get

$$\frac{V_P}{V_N} = \frac{N_D}{N_A} \quad ...(3.20)$$

Since $N_D >> N_A$, it indicates that $V_P >> V_N$ *i.e., potential change is confined to the lightly doped region.*

The density of electrons in conduction band in an intrinsic semiconductor is given by

$$n = n_c = 2\left[\frac{2\pi m_e k_B T}{h^2}\right]^{3/2} e^{(E_F - E_C)/k_B T} \quad ...(3.21)$$

Addition of donor impurity raises the Fermi level by ΔE on N-side, so that now Fermi level is

$$E_F' = E_F + \Delta E$$

and expression for density of electrons on N-side modified to

$$(n_c)_N = 2\left[\frac{2\pi m_e k_B T}{h^2}\right]^{3/2} e^{(E_F + \Delta E - E_C)/k_B T}$$

or
$$(n_c)_N = n e^{\Delta E/k_B T} \quad ...(3.22)$$

Similarly, the density of electrons on P-side is given by

$$(n_c)_p = n e^{(-\Delta E'/k_B T)} \quad ...(3.23)$$

because addition of donor impurities brings down the Fermi level on P-side by $\Delta E'$.

From Eqs. (3.22) and (3.23), we get

$$\frac{(n_c)_N}{(n_c)_P} = e^{(\Delta E + \Delta E')/k_B T} = e^{(eV_B/k_B T)} \quad \text{...(3.24)}$$

where V_B is the height of potential barrier and

$$eV_B = \Delta E + \Delta E'$$

From Eq. (3.24), we have $$V_B = \frac{k_B T}{e} \log_e \frac{(n_c)_N}{(n_c)_P} \quad \text{...(3.25)}$$

But the intrinsic density n_i of either carrier (regardless of donor or acceptor concentrations) for a semiconductor is given by the law of mass action

$$n_c(n_h + N_D) = n_i^2$$

For a semiconductor having N_D completely ionised donor atoms, it becomes

$$(n_c' + N_D)n_h' = n_i^2$$

where n_c' and n_h' are the number of thermally generated electron-holes.

For *N*-type semiconductor, $N_D > n_c'$ and we have

$$N_D n_h' = n_i^2$$

Therefore the hole concentration in *N*-type semiconductors *i.e.*, minority carrier concentration

$$(n_h')_N = \frac{n_i^2}{N_D} \quad \text{...(3.26)}$$

Similarly, for a semiconductor having N_A completely ionised acceptor atoms

$$n_c'(N_A + n_h') = n_i^2$$

But for a *P*-type semiconductor $N_A > n_h'$ and we have

$$n_c' N_A = n_i^2$$

Therefore, electron concentration in *P*-type material

$$(n_c')_P = \frac{n_i^2}{N_A} \quad \text{...(3.27)}$$

If we assume that minority carriers on *P*-side are thermally generated, then

$$(n_c')_P = \frac{(n_c)_P}{N_A} \quad \text{...(3.28)}$$

Using Eqs. (3.28), (3.27) and (3.25), we get

$$V_B = \frac{k_B T}{e} \log_e \left[\frac{(n_c)_N}{n_i^2 / N_A} \right] \quad \text{or} \quad V_B = \frac{k_B T}{e} \log_e \left[\frac{(n_c)_N N_A}{n_i^2} \right] \quad \text{...(3.29)}$$

Since majority carriers (electrons) in *N*-type semiconductor are largely contributed by donor atoms, we take

$$(n_e)_N = N_D$$

Therefore, Eq. (3.29) becomes

$$V_B = \frac{k_B T}{e} \log_e \left(\frac{N_D N_A}{n_i^2} \right) \qquad ...(3.30)$$

This gives the height of barrier potential in terms of impurity densities that create it.

Example 3.1 *Calculate the width of depletion layer of a PN-junction of depletion layer of a PN-junction of* $N_D = N_A = 10^{21}/m^3$, $V_B = 0.2$ *V and* $\varepsilon_r = 10$.

Solution. Here we consider $N_A = N_D$, then width of depletion layer

$$x = \left[\frac{4\varepsilon_r \varepsilon_0 V_B}{eN_D} \right]^{1/2}$$

$$= \left[\frac{4 \times 10 \times 8.85 \times 10^{-12} \times 0.2}{1.6 \times 10^{-19} \times 10^{21}} \right]^{1/2} = \left[\frac{8 \times 8.85}{1.6} \times 10^{-14} \right]^{1/2}$$

$$= (5 \times 8.85)^{1/2} \times 10^{-7} = (44.24)^{1/2} \times 10^{-7} \text{ m}$$

$$x = 6.64 \times 10^{-7} \text{ m} = 0.664 \, \mu\text{m}$$

Example 3.2 *In a PN-junction diode,* $N_A = N_D = 10^{21}/m^3$ *and* $n_i = 2.5 \times 10^{19}/m^3$. *Calculate the barrier potential.*

Solution. We know that barrier potential, $V_B = \frac{k_B T}{e} \log_e \frac{N_A N_D}{h_i^2}$

$$\frac{k_B T}{e} = 0.026 \text{ V}$$

$$V_B = 0.026 \log_e \left(\frac{N_A}{n_i^2} \right)^2 = 0.052 \log_e \frac{N_A}{n_i}$$

$$= 0.052 \log_e \frac{10^2}{2.5 \times 10^{19}} = 0.052 \log_e 40 = 0.052 \times 2.303 \times \log_{10} 40$$

$$= 0.052 \times 2.303 \times 1.6021 = 0.167 \text{ V}$$

3.2.2 Forward and Reverse Biased *PN*-junctions

In order to obtain a current through the junction, the potential barrier across the junction has to be neutralized. This is done by applying an external potential across the two ends of the crystal, so that it opposes the junction potential as shown in Fig. 3.11. The voltage applied in this manner *i.e.*, by connecting the positive terminal of external battery to the *P*-region and negative terminal to the *N*-region, is called a *forward bias*. Forward bias applied to a *PN*-junction facilitates the

been reduced so that a portion of the a... junction is crossed, a number of electrons and holes will combine that will cease to exist as mobile charge carriers. For each hole in the *P*-section that combines with an electron from the *N*-section, a covalent bond near the positive battery terminal breaks down and an electron is liberated which enters the positive terminal. This action creates a new hole, which moves towards the junction under the force of the applied e.m.f.

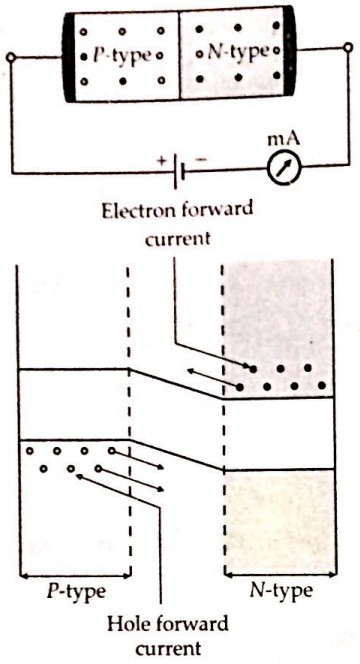


Figure 3.11 Forward biased PN-junction diode.

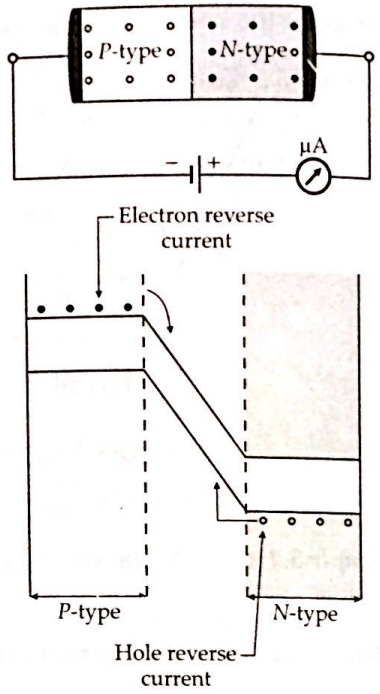


Figure 3.12 Reverse biased *PN*-junction diode.

In the *N*-region where the electrons combine with equal number of holes from the *P*-region, equal number of electrons arrive from the negative terminal of the battery and enter the *N*-region to replace the electron lost by combination with holes near the junction. These electrons move towards the junction at the left, where they again combine with new holes arriving there. This process thus goes on and maintains the continuity of current flow of relatively large value.

It should be noted that the current in the *N*-region, the external connecting wires and battery, is carried by the electrons, whereas in the *P*-region, the current is carried by holes. As we approach in the vicinity of the *PN*-junction, we get both the types of carriers.

If the external battery voltage is reversed in polarity, so that the negative terminal of the battery is now connected to the *P*-region and the positive terminal is connected to the *N*-region as shown in Fig. 3.12, an entirely different saturation prevails. This connection gives a reversed biased junction and it has the effect of increasing the potential barrier across the junction and width of the depletion area as shown in Fig. 3.12. The excess holes in the *P*-region are now attracted to the negative terminal of the battery and move away from the *PN*-junction.

At the same time the free electrons in the *N*-region are attracted by the positive battery terminal and also move away from the *PN*-junction. There can be no significant recombination, and the junction resistance appears high. The only possible current results from the few minority carriers on each side of the junction. The magnitude of this reverse current is dictated primarily by the junction temperature, because major source of minority carriers is thermally broken covalent bonds. Electrons liberated by this process in the *P*-region move right across the junction under the influence of the electric field and as they enter the *N*-region, an equal number of electrons enter the *P*-region from the negative battery terminal. Similarly, the holes generated in the *N*-region move to the left into the *P*-region, where they receive electrons and combine with them. For each such combination, one electron leaves a covalent bond in the crystal near the positive terminal of the battery. A new hole is thus created which moves across the junction under the influence of applied e.m.f. In fact the situation here is exactly similar to that discussed earlier when the *PN*-junction was forward biased and the majority carriers were involved.

3.2.3 Voltage-Current (V-I) Characteristics of *PN*-Junction Diode

The *V-I* characteristic of a *PN*-junction diode is the curve between voltage across the junction (taken along *X*-axis) and current (taken along *Y*-axis) and has been shown in Fig. 3.13 for germanium and silicon diodes. These characteristics are called the *static characteristics* because they describe the d.c. behaviour of the diode.

When the *PN*-junction is forward biased by connecting positive terminal of battery to *P*-type and negative terminal to *N*-type, the potential barrier is reduced. Practically no current flows until the barrier voltage (0.3 V for Ge and 0.7 V for Si) is overcome. Then the curve has a linear rise and the current increases, with the increase in forward voltage like an ordinary conductor. With the applied voltage of about 3 V, the majority charge carriers are passing the junction gain sufficient kinetic energy to knock out valence electrons bound to the crystal lattice and raise them to the conduction band. Therefore, the forward current then increases sharply as shown in Fig. 3.13.

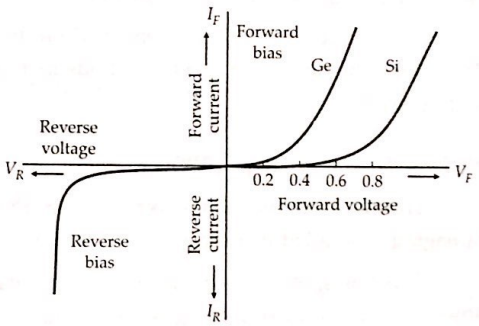


Figure 3.13 Characteristic curve of a *PN* junction diode.

With reverse bias *i.e.*, when positive terminal of external battery is connected to *N*-type and negative terminal to *P*-type, the potential barrier at the junction increased. Consequently, the junction resistance becomes very high which prevents the flow of current. However, a few minority charge carriers (free electrons in *P*-type material and holes in *N*-type material) are accelerated by the reverse bias voltage resulting in a very small current (of the order of μA) in the circuit. When reverse voltage is increased beyond a value called *breakdown voltage*, the reverse current increases suddenly and sharply and the diode shows almost zero resistance. It is known as "*avalanche breakdown*" and is due to the fact that at a reverse voltage about 25 V, the excessively high temperature destroys the junction permanently.

3.3 Limitations in the Operating Conditions of *PN*-junction

When a diode is biased with a voltage more than its *knee voltage*, there is a large current flow. Because of this large current, heat is produced at the diode junction. If this heat produced is large as compared to what the diode can withstand, the junction burns out and the diode gets damaged. For this reason, it is always advisable to operate a diode below the maximum power rating given by manufacturer.

Under reverse bias conditions, there is a very small current in the diode. When enough reverse voltage is applied, the diode current begins to increase sharply. This voltage is known as *breakdown voltage of the diode*. At this voltage if the current through the diode is not checked , the diode may burn out.

Every *PN*-junction has limiting values of :

- Maximum forward current
- Peak inverse voltage (PIV)
- Maximum power rating

(*i*) Maximum Forward Current

The maximum value of forward current that a *PN*-junction (or diode) without damaging itself is called its *maximum forward current*.

This rating of a *PN* junction or diode is specified by the manufacturer in its data sheet. However, if the forward current in a diode increased beyond this specified value, the junction will be destroyed.

(*ii*) Peak Inverse Voltage (PIV)

The maximum value of reverse voltage that a *PN*-junction (or diode) can withstand without damaging it is called its *peak inverse voltage* (PIV).

This rating of a *PN* junction or diode is also specified by the manufacturer in its data sheet. However, if the voltage coming across the junction at reverse bias condition increases beyond the specified value, the junction will be destroyed.

(*iii*) Maximum Power Rating

The maximum power that a *PN*-junction (or diode) can dissipate without damaging it is called its *maximum power rating*.

Usually, it is specified by the manufacturer in its data sheet. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction. If the power developed across the junction is more than the maximum power dissipated by it, the junction will be overheated and may be destroyed. It may be noted here that more often, the data sheets list only the maximum current that a diode can handle since it is more convenient to measure and to design with.

3.4 Diode Current Equation

The current flowing through a *PN*-junction diode due to the application of a voltage V across the junction is given by

$$I = I_0[e^{Ve/\eta k_B T} - 1] \quad ...(3.31)$$

where I_0 = reverse saturation current in Ampere at temperature T K,

e = electronic charge $= 1.6 \times 10^{-19}$ C,

k_B = Boltzmann constant $= 1.38 \times 10^{-23}$ J/K,

T = Temperature in K,

and η = Constant which depends upon the material of the diode. (It is 1 for Ge and 2 for Si).

For a forward biased junction. V is positive. For large forward biased voltage, $e^{Ve/\eta k_B T} > 1$. Hence, unity within the bracket in Eq. (3.31) can be neglected and we have

$$I_F = I_0 e^{Ve/\eta k_B T} \quad ...(3.32)$$

Thus forward current I_F increases exponentially with voltage V except for very small values of V.

When Diode is reverse biased. V is negative and Eq. (3.31) takes the from

$$I_R = I_0\left[\frac{1}{e^{Ve/\eta k_B T}} - 1\right] \quad ...(3.33)$$

For larger reverse bias voltage, exponential term quickly becomes negligible with respect to unity. Then

$$I_R \approx -I_0 \quad ...(3.34)$$

Thus reverse current I_R is constant independent of applied reverse bias.

Derivation

To determine the current-voltage relationship for the biased *PN*-junction, the concentration of electrons in the *N*-region

$$n_N = 2\left[\frac{2\pi m_n^* k_B T}{h^2}\right]^{3/h} e^{-(E_{CN} - E_{FN})/k_B T} \quad ...(3.35)$$

where m_n^* = effective mass of electron in the conduction band,

E_{CN} = energy at the bottom of conduction band,

and E_{FN} = Fermi level

The *P*-region also contains some thermally generated electrons of concentration

$$n_P = 2\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{3/2} e^{(E_{CP} - E_{FP})/k_B T} \quad ...(3.36)$$

If we divide Eq. (3.35) by Eq. (3.36), we get

$$\frac{n_N}{n_P} = \frac{e^{-(E_{CN}-E_{FN})/k_BT}}{e^{-(E_{CP}-E_{FP})/k_BT}} \quad ...(3.37)$$

For the same semiconducting material, the positions of the conduction and valence band edges do not change with doping, whereas the position of the Fermi level changes with both concentration and type of doping. Thus for N and P regions

$$E_{CN} = E_{CP} \text{ and } E_{FN} \neq E_{FP}$$

Therefore Eq. (3.37) reduces to

$$\frac{n_N}{n_P} = e^{(E_{FN}-E_{FP})/k_BT} = e^{(eV_B/k_BT)} \quad ...(3.38)$$

where $E_{FN} - E_{FP} = eV_B = E_B$, is the *barrier energy* and V_B is the difference in potentials in the two regions, known as *barrier potential*.

Thus at equilibrium, the minority carrier electron concentration in the P-region is related to the majority carrier electron concentration in the N-region by

$$n_P = n_N e^{(-eV_B/k_BT)} \quad ...(3.39)$$

On applying a small forward voltage V, the effective barrier potential decreases to $(V_B - V)$ and some of the majority carriers diffuse across the junction. Thus holes diffuse to N-side and the electron to P-side. Consequently, minority carrier electron concentration at the edge of transition region on the P-side becomes greater than its equilibrium value by a small amount Δn_p. The majority carrier electron concentration in the N-region, however, remains nearly constant. Hence for applied forward bias, Eq. (3.39) takes the form

$$\begin{aligned} n_P + \Delta n_P &= n_N e^{-e(V_B-V)/k_BT} \\ &= n_P e^{(eV_B)/k_BT}\, e^{-e(V_B-V)/k_BT} \quad \text{[Using Eq. (3.38)]} \\ &= n_P e^{eV/k_BT} \end{aligned}$$

or
$$\Delta n_P = n_P[e^{eV/k_BT} - 1] \quad ...(3.40)$$

Similarly, for excess holes on the N-side

$$\Delta p_N = p_N[e^{eV/k_BT} - 1] \quad ...(3.41)$$

The diffusion currents produced by those charges can be determined by using diffusion equations and *Fick's first law*. The electron diffusion current injected into the P-region at the junction is given by

$$I_N = \frac{eAD_N}{L_N}\Delta n_P = \frac{eAD_N}{L_N} n_P[e^{eV/k_BT} - 1] \quad ...(3.42)$$

where A = area of cross-section of the junction in m^2,

D_N = diffusion coefficient of electron in m^2/s,

and L_N = electron diffusion length (average distance an electron diffuses before recombining with the opposite type of carrier)

Similarly, the hole diffusion current injected into the N-region at the junction is

$$I_p = \frac{eAD_p}{L_p} p_N [e^{eV/k_BT} - 1] \quad ...(3.43)$$

where D_p = Diffusion coefficient and L_p = Diffusion length

Since the direction of both the currents is the same, the total diode current

$$I = I_P + I_N = eA\left[\frac{D_p}{L_p} p_N + \frac{D_N}{L_N} n_p\right](e^{eV/k_BT} - 1) = I_0[e^{eV/k_BT} - 1] \quad ...(3.44)$$

where

$$I_0 = eA\left[\frac{D_p}{L_p} p_N - \frac{D_N}{L_N} n_p\right] \quad ...(3.45)$$

Equation (3.44) is called the *Diode Current Equation*, where I_0[given by Eq. (3.45)] is called reverse saturation current.

The empirical form of Eq. (3.44) is

$$I = I_0[e^{eV/\eta k_BT} - 1] \quad ...(3.46)$$

where η is a numerical constant, which depends upon the material of diode. Its value is 1 for Ge and 2 for Si.

Example 3.3 *A P-N junction silicon diode conducts 240 mA current when a forward voltage 0.8 volts is applied. Find :*

(i) Current for forward voltage of 0.7 volts. *(ii) Reverse saturation current.*

Solution. (*i*) From junction diode equation

$$I = I_0[e^{Ve/\eta k_BT} - 1] = I_0[e^{V/\eta V_T} - 1]$$

where V_T (Volt equivalent of temperature) is given by

$$V_T = \frac{k_BT}{e} = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \text{ V}$$

at room temperature (300 K)

$$V_T = 0.026 \text{ volt} \qquad \because \quad \eta = 2 \text{ for silicon}$$

$$I \approx I_0 e^{[0.8/(2\times0.026)]} \quad \text{and} \quad I' = I_0[e^{0.7/(2\times0.026)}]$$

$$\therefore \quad \frac{I'}{I} = \exp\left[\frac{0.7 - 0.8}{2 \times 0.026}\right] = 35 \text{ mA}$$

(*ii*) From *diode equation*

$$240 \times 10^{-3} = I_0[e^{0.8/0.052} - 1]$$

or

$$I_0 = \frac{240 \times 10^{-3}}{4.8 \times 10^6} = 50 \times 10^{-9} \text{ A} = 50 \text{ nA}$$

Example 3.4 *The saturation current density of a P-N junction germanium diode is 200 mA/m^2 at 27° C. Find the voltage to be applied across the junction to have forward current density of 10^4 A/m^2 to flow.*

Solution. The diode current for germanium at a temperature T is given by

$$I = I_0\left[\exp\frac{eV}{k_BT} - 1\right]$$

$$J = J_0\left[\exp\frac{eV}{k_BT} - 1\right]$$

or $$\frac{J}{J_0} = \exp\frac{eV}{k_BT} - 1 \qquad \text{or} \qquad \frac{eV}{k_BT} = \ln\frac{J}{J_S}$$

With $J = 10^4\,A/m^2$, $J_0 = 200\times10^{-3}\,A/m^2$, $e = 1.6\times10^{-19}\,C$,

$k_B = 1.38\times10^{-23}\,J/K$, $T = 27°C = 300\,K$

i.e., $$V = \frac{k_BT}{e}\ln\frac{J}{J_0} = \frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}}\ln\frac{10^4}{200\times10^{-3}} = 0.28\ V$$

Example 3.5 *For what voltage will the reverse current in a P-N junction germanium diode attain a value of 90% of its saturation value at room temperature ?*

Solution. Give $I = 90\%$ of I_0, $T = 300\,K$, $V = ?$

The general form of the rectifier equation is

$$I = I_0\left[\exp\frac{eV}{k_BT} - 1\right]$$

or $$\frac{I}{I_0} = \exp\frac{eV}{k_BT} - 1 \qquad \text{or} \quad 0.9 = \exp\frac{eV}{k_BT}$$

or $$\frac{eV}{k_BT} = \ln 0.9$$

or $$V = \frac{\ln 0.9\times k_BT}{e} = \frac{\ln 0.9\times1.38\times10^{-23}\times300}{1.6\times10^{-19}} = 0.017\ V$$

3.5 Effect of Temperature on *PN*-Junction Diode Characteristics

The temperature can have a marked effect on the characteristics of silicon semiconductor diode as shown in Fig. 3.14. It has been observed experimentally that :

(i) The reverse saturation current I_0 will just about double in magnitude for every 10°C increase in temperature.

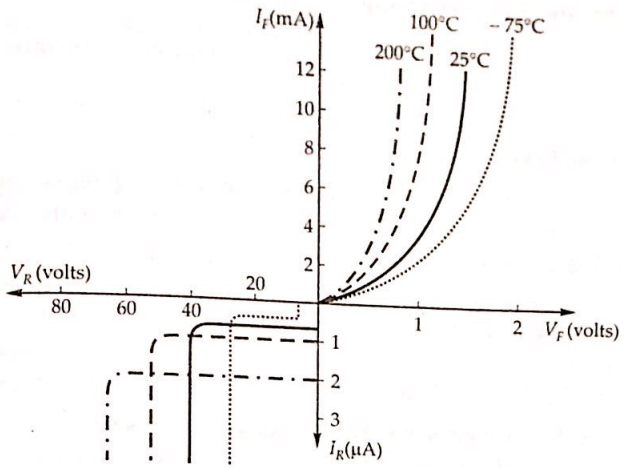


Figure 3.14 Variation in diode characteristics with temperature.

(*ii*) The increasing levels of I_0 with temperature account for the lower levels of threshold voltage.

Typical values of I_0 for silicon are much lower than that of germanium for similar power and current levels. This result is that even at high temperatures the levels of I_0 for silicon diodes do not reach the same high levels obtained for germanium. *This is also one of the reasons that silicon device enjoys significantly higher level of development and utilization in design.*

(*iii*) If $I_0 = I_{01}$ at temperature T_1, then at any temperature T, the value of reverse saturation current I_0 is given by

$$I_0(T) = I_{01} \times 2^{(T-T_1)/10} \qquad ...(3.47)$$

(*iv*) For either silicon or germanium (at room temperature) it is found that

$$\frac{dV}{dT} = -2.5 \text{ mV/°C} \qquad ...(3.48)$$

in order to maintain a constant value of I.

Example 3.6 *Find the increase in temperature ΔT necessary to increase I_0 by a factor of* 100.

Solution. As the reverse saturation current I_0 of a Si diode and Ge diode approximately doubled for every 10° C rise in temperature, therefore,

$$\frac{I_{02}}{I_{01}} = 100 = 2^{(T_2-T_1)/10} = 2^{\Delta T/10}$$

or

$$\Delta T = \frac{10 \ln 100}{\ln 2} = \frac{10 \times 2}{0.310} = 66.4° \text{C}$$

3.6 Breakdown in *PN*-Junction Diode

With reverse bias voltages, the following two mechanisms are responsible for breakdown in a *PN*-junction diode :

3.6.1 Avalanche Breakdown

In this mechanism, the minority charge carriers (electrons in *P*-region and holes in *N*-region) gain large kinetic energy from the applied reverse voltage to collide with valence electrons of the atom fixed in the crystal and liberate them. Thus, in this process, covalent bonds are broken and pairs of electrons and holes are generated. The new carriers so produced, in turn, generate new additional carriers and thus the number of free electrons and holes goes on increasing. This cumulative phenomenon is called *avalanche breakdown multiplication* and produces a sharp increase in the reverse current. The diode is then said to be in the avalanche breakdown region.

The magnitude of the avalanche breakdown voltage increases with increase in temperature. As the temperature increased, the amplitude of vibration of crystal atoms increases which increases the probability of collision of the carriers with the crystal atoms. Consequently, there will be loss of energy of the carriers and therefore, the applied reverse voltage should be increased to make up the loss of energy and to start avalanche process.

3.6.2 Zener Breakdown

The Zener breakdown occurs in junctions, which are heavily doped and have a very narrow depletion region, of the order of 150 – 200 Å. Thus, there exists a high electric field, of the order of 10^8 V/m across the junction. This field is strong enough to break or rupture the covalent bonds thereby generating electron-hole pairs. Even a small further increase in reverse voltage is capable of producing large number of current carriers. The *Zener breakdown* is, thus, a *"field emission"* phenomenon, the strong electric field in the junction region pulling carriers from their atoms.

In order to study the effect of temperature on breakdown phenomenon, we see that an increase in temperature increases the energies of the valence electrons and hence makes it easier for these electrons to escape from the covalent bonds. Less applied voltage is therefore, required to pull these electrons from their positions in the crystal lattice and convert them into conduction electrons. The Zener breakdown voltage, therefore, decreases with an increase in temperature.

3.7 Diode Resistance

Since the forward and reverse characteristics of a semiconductor diode are non-linear, the resistance offered by the device will be different at different operating points. The semiconductor diode resistance is of *three* different kinds :

- DC resistance or static resistance
- AC resistance or dynamic resistance
- AC average resistance.

3.7.1 DC Resistance or Static Resistance

The resistance of a diode at a particular operating point is called the dc or static resistance of the diode.

It is defined as the ratio of the dc voltage across the diode to the resulting dc current flowing through it.

Mathematically, the static resistance is given by

$$R_{dc} = \frac{V_F}{I_F} \qquad ...(3.49)$$

Now referring to Fig. 3.15, for the operating point Q_1, the static forward resistance is given by d.c. forward $R_{dc} = \frac{OA_1}{OB_1}$

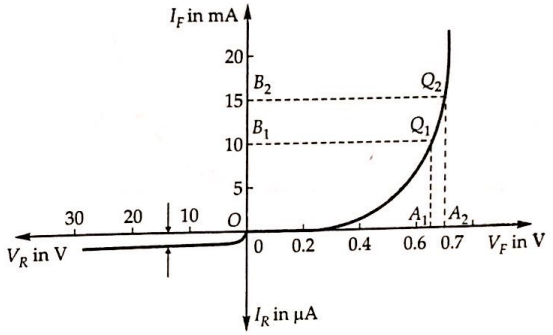


Figure 3.15 Determination of dc resistance of diode at different operating points

At point Q_1, $$R_{dc} = \frac{OA_1}{OB_1} = \frac{0.65\text{ V}}{10\text{ mA}} = 65\Omega$$

At point Q_2, $$R_{dc} = \frac{OA_2}{OB_2} = \frac{0.7\text{ V}}{15\text{ mA}} = 46.67\,\Omega$$

The results clearly show that the dc resistance of a diode in the forward bias region decreases as we approach the region of higher currents and voltages.

In the reverse bias region at $V_R = -10$ V the resistance of the diode is given by

$$R_{dc} = \frac{-10\text{ V}}{-2\,\mu\text{A}} = 5\,\text{M}\Omega$$

which is certainly equivalent to an open circuit for many applications.

3.7.2 AC Resistance or Dynamic Resistance

The resistance offered by the diode in the forward bias to an ac signal is called *dynamic resistance*. The ac resistance of a diode at a particular dc voltage is equal to the reciprocal of the slope of the characteristics at that point.

It is defined as the ratio of small change in forward voltage to the corresponding change in the diode current.

Mathematically, the ac forward resistance is given by

$$\text{ac forward resistance } R_{ac} = \frac{\Delta V_F}{\Delta I_F} \qquad \ldots(3.50)$$

In order to find ac resistance of a diode, choose any two points M and N on either side of the operating point Q_1 at equal distances as shown in Fig. 3.16.

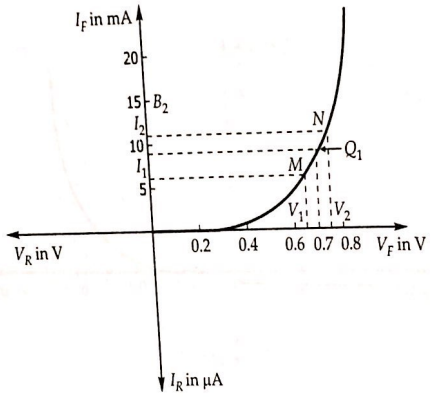


Figure 3.16 Determination of ac resistance of a diode from *V-I* characteristics.

If V_1 and V_2 are the voltages and I_1 and I_2 the currents corresponding to M and N, then

$$\text{ac resistance, } R_{ac} = \frac{V_2 - V_1}{I_2 - I_1} = \frac{\Delta V_F}{\Delta I_F}$$

The steeper the slope, the lesser the value of ΔV_F for the same range in ΔI_F and the lower the resistance. The ac resistance in the vertical rise region of the characteristic is therefore quite small while the ac resistance is much higher at low current levels.

The value of ac resistance of a diode is therefore small, ranging 1 to 25 Ω.

3.7.3 Average AC Resistance

If the input signal is sufficiently large to produce the type of swing shown in Fig. 3.17, the resistance associated with the device for this region is called the ac average resistance. The operating point Q swings between the linear and non-linear regions as shown in Fig. 3.17. The average ac resistance by definition, the resistance determined by the straight line drawn between the two intersections determined by the maximum and minimum values of input voltages.

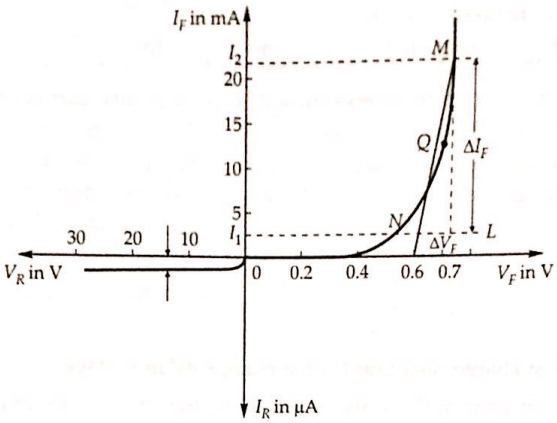


Figure 3.17 Determination of average ac resistance of the diode.

Hence $$R_{av} = \frac{\Delta V_F}{\Delta I_F} \qquad ...(3.51)$$

It is important to note that the resistance to be associated with the element is determined only by region of intersect, not by the entire characteristic.

Example 3.7 *From the forward and reverse bias characteristics of an ideal diode as shown in Fig. 3.18, determine (a) dc resistance at $I_F = 40$ mA, (b) ac resistance at $I_F = 30$ mA and (c) reverse saturation current.*

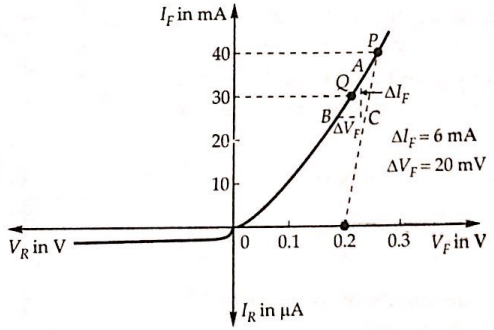


Figure 3.18

Solution. (*a*) DC resistance at a point P where $I_F = 40$ mA is given by

$$R_{dc} = \frac{V_F}{I_F} = \frac{0.2}{40 \times 10^{-3}} = 5\Omega$$

(*b*) AC resistance at point Q where $I_F = 30$ mA is given by

$$R_{ac} = \frac{\Delta V_F}{\Delta I_F} = \frac{20 \times 10^{-3}}{6 \times 10^{-3}} = 3.33\,\Omega$$

(*c*) From the reverse characteristic curve, it is found that reverse saturation current $I_0 = 2\,\mu A$.

(*i*) Step Graded Junction

Figure 3.19 shows the net charge density as a function of distance from the junction. Let us assume that acceptor impurity density N_A is much greater than the donor impurity density N_D.

Since the net charge in the device must be zero, we get

$$eN_A W_P = eN_D W_N \qquad ...(3.53)$$

where e is the magnitude of the charge of an electron. According to our assumption, $N_A >> N_D$, this means according to above equation $W_P << W_N$. Hence for simplification, neglecting W_P and assuming that entire barrier potential V_j drops across the region W_N of the uncovered donor ions.

Using Poisson's equation, we have

$$\frac{d^2V}{dx^2} = -\frac{eN_D}{\varepsilon} \qquad ...(3.54)$$

where ε is the absolute permittivity of the semiconductor integrating Eq. (3.54), we get

$$\frac{dV}{dx} = \frac{-eN_D}{\varepsilon} x + C_1 \qquad ...(3.55)$$

Now using boundary conditions, that at

$$x = W_N \cong W$$

$$-\frac{dV}{dx} = 0 = E$$

This gives $$C_1 = \frac{eN_D W}{\varepsilon}$$

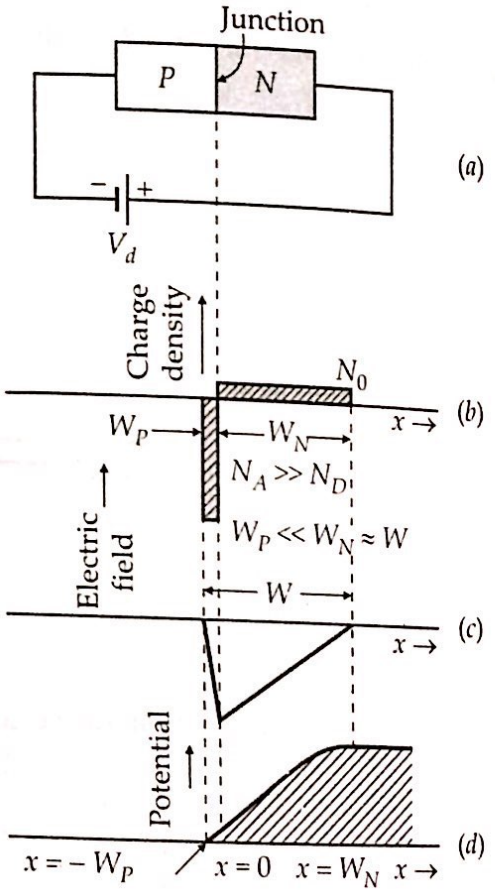
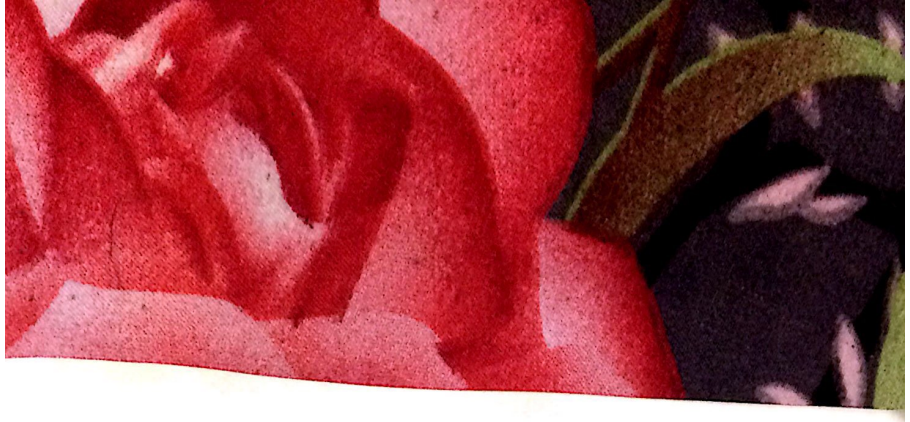


Figure 3.19 (*a*) Reversed biased step graded *PN* junction. (*b*) Charge density *vs.* distance curve. (*c*) Electric field *vs.* distance curve. (*d*) Potential *vs.* distance curve.



Then Eq. (3.55) may be written as

$$\frac{dV}{dx} = -\frac{eN_D}{\varepsilon}(x - W) = -E \qquad \ldots(3.56)$$

Again integrating Eq. (3.56), we get

$$V = -\frac{eN_D}{\varepsilon}\left[\frac{x^2}{2} - Wx\right] + C_2 \qquad \ldots(3.57)$$

Neglect small drop in potential across W_p, we use the boundary condition $V = 0$ at $x = 0$. Hence Eq. (3.57) may be written as

$$V = -\frac{eN_D}{\varepsilon}\left[\frac{x^2}{2} - Wx\right] \qquad \ldots(3.58)$$

At $x = W_N (\approx W)$, $V = V_j$ = junction or barrier potential

$$V_j = \frac{eN_D W^2}{2\varepsilon} \qquad \ldots(3.59)$$

Also $$V_j = V_0 - V_d$$

where V_d is a negative number indicating the applied reverse bias and V_0 is the contact potential.

Hence in case of step-graded junction, the width W of the junction varies as $V_j^{1/2}$

i.e., $$W \propto V_j^{1/2} \qquad \ldots(3.60)$$

Thus we conclude that the thickness W of the depletion layer increases with the increase in applied reverse bias magnitude V_d.

Let A be the area of the junction. Then the total charge in the distance W of the depletion layer is

$$Q = eN_D W_A \qquad \ldots(3.61)$$

Hence the transition capacitance C_T is given by

$$C_T = \left|\frac{dQ}{dV_j}\right| = eN_D A \left|\frac{dW}{dV_j}\right| \qquad \ldots(3.62)$$

From Eq. (3.59), we have

$$W^2 = \frac{2\varepsilon V_j}{eN_D}$$

$$\therefore \quad 2W\frac{dW}{dV_j} = \frac{2\varepsilon}{eN_D}$$

or $$\left|\frac{dW}{dV_j}\right| = \frac{\varepsilon}{eN_D W} \qquad \ldots(3.63)$$

On substituting Eq. (3.63) in Eq. (3.62), we get

$$C_T = eN_D A \frac{\varepsilon}{eN_D W}$$

or
$$C_T = \frac{\varepsilon A}{W} \quad \text{...(3.64)}$$

From Eq. (3.64), we conclude that the transition capacitance C_T is exactly the same as the capacitance of a parallel plate capacitor having plate area $A(\text{m}^2)$ and plate separation $W(\text{m})$ containing materials of permitivity ε.

In case of the donor concentration N_D is not neglected in comparison with the acceptor concentration N_A, Eq. (3.59) becomes

$$V_j = \frac{e(W_P - W_N)^2}{2\varepsilon\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \quad \text{...(3.65)}$$

(ii) Linearly Graded Junction

In the linearly graded junction, the net charge density in the transition region varies linearly with distance and becomes zero abruptly at the edges distant $+\frac{W}{2}$ and $-\frac{W}{2}$ as shown in Fig. 3.20.

Thus we may write net charge density.

$$\rho = ekx \left(\frac{-W}{2} < x < \frac{W}{2}\right) \quad \text{...(3.66)}$$

where k = proportionality constant, e = magnitude of the charge on electron.

Using Poisson's equation

$$\frac{d^2V}{dx^2} = -\frac{ekx}{\varepsilon} \quad \text{...(3.67)}$$

where V is the potential at a point distant x from the origin.

Integrating Eq. (3.67), we get

$$\frac{dV}{dx} = -\frac{ek}{\varepsilon}\frac{x^2}{2} + C_1 \quad \text{...(3.68)}$$

But at $x = \pm\frac{W}{2}$, electric field $E = -\frac{dV}{dx} = 0$

This yields $0 = \frac{-ek}{\varepsilon}\frac{W^2}{8} + C_1$

or
$$C_1 = \frac{ekW^2}{8\varepsilon}$$

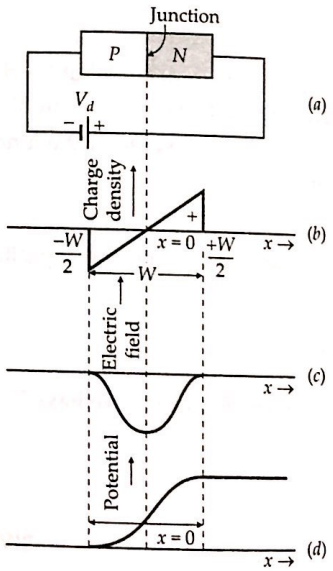


Figure 3.20 (*a*) Reverse biased linearly graded *PN*-junction, (*b*) charge density *vs.* distance curve (*c*) Electric field *vs.* distance curve (*d*) potential *vs.* distance curve.

Hence Eq. (3.68) becomes

$$\frac{dV}{dx} = -\frac{ek}{\varepsilon}\left[\frac{x^2}{2} - \frac{W^2}{8}\right] \qquad ...(3.69)$$

Integrating Eq. (3.69), we get

$$V = -\frac{ek}{\varepsilon}\left[\frac{x^3}{6} - \frac{W^3}{8}x + C_2\right] \qquad ...(3.70)$$

At $x = 0, W = 0$, this yields $C_2 = 0$

$$\therefore \quad V = -\frac{ek}{2\varepsilon}\left[\frac{x^3}{3} - \frac{W^2 x}{4}\right] \qquad ...(3.71)$$

Figure 3.20(*c*) shows the variation of the electric field with distance while Fig. 3.20(*d*) shows the variation of potential V as a function of distance across the transition region.

The total potential V_j across the junction is given by

$$V_j = V_{\left(x=\frac{W}{2}\right)} - V_{\left(x=\frac{-W}{2}\right)}$$

$$= -\frac{ek}{2\varepsilon}\left[\frac{W^3}{24} - \frac{W^3}{8}\right] + \frac{ek}{2\varepsilon}\left[-\frac{W^3}{24} + \frac{W^3}{8}\right] = \frac{ekW^3}{12\varepsilon} \qquad ...(3.72)$$

where $V_j = V_0 - V_d$.

Hence in case of linearly graded junction

$$W \propto V_j^{1/3} \qquad ...(3.73)$$

In linearly graded junction also, the thickness W of the depletion region increases with increase of applied reverse bias magnitude V_d.

Let A be the area of the junction. Then the total charge in one side of the depletion layer is

$$Q = \frac{1}{2}\left(\frac{W}{2}\right)\left(\frac{ekW}{2}\right)A$$

or

$$Q = \frac{ekW^2 A}{8} \qquad ...(3.74)$$

Hence the transient capacitance C_T is given by

$$C_T = \left|\frac{dQ}{dV_j}\right| = \frac{AekW}{4}\left|\frac{dW}{dV_j}\right| \qquad ...(3.75)$$

From Eq. (3.72)

$$\frac{12\varepsilon}{qk} = 3n^2\frac{dW}{dV_j}$$

$$\therefore \quad \frac{dW}{dV_j} = \frac{4\varepsilon}{ekW^2} \qquad ...(3.76)$$

Hence Eq. (3.75) becomes

$$C_T = \frac{AekW}{4} \times \frac{4\varepsilon}{ekW^2} = \frac{\varepsilon A}{W} \qquad ...(3.77)$$

Thus we get the same expression for C_T in case of both step graded junction and linearly graded junction.

To calculate the maximum field strength within the junction, taking Eq. (3.69)

$$E = -\frac{dV}{dx} = \frac{ek}{\varepsilon}\left[\frac{x^2}{2} - \frac{W^2}{8}\right] \qquad ...(3.78)$$

At $x = 0$, field is maximum

$$E_{max} = \frac{ekW^2}{8\varepsilon} \qquad ...(3.79)$$

Combining Eqs. (3.72) and (3.79), we get

$$W = \left(\frac{12\varepsilon V_j}{ek}\right)^{1/3}$$

$$\therefore \quad E_{max} = \frac{ek}{8\varepsilon}\left(\frac{12\varepsilon V_j}{ek}\right)^{2/3} \qquad ...(3.80)$$

and

$$C_T = \frac{\varepsilon A}{\left(\frac{12\varepsilon V_j}{ek}\right)^{1/3}} \qquad ...(3.81)$$

Thus C_T is inversely proportional to one-third power of V_j.

3.9 Diffusion Capacitance (C_D)

When a *PN*-junction diode is forward biased, diode offers a capacitance caused by the injected charge stored near the junction just outside the transition region, this capacitance is called as *diffusion capacitance* C_D. This is also termed as storage capacitance.

C_D may also be defined as the rate of change of injected charge with voltage

$$C_D = \frac{dQ}{dV} = \tau\frac{dI}{dV} = \tau g_m = \frac{\tau}{r} \qquad ...(3.82)$$

where g_m is the diode incremental conductance and equals $\frac{dI}{dV}$, r is the dynamic resistance $= \frac{\eta V_T}{I}$.

$$C_D = \frac{\tau I}{\eta V_T} \qquad ...(3.83)$$

where $V_T = \frac{k_B T}{e}$. Thus, the diffusion capacitance is proportional to I.

For Forward Bias :

C_D is usually much greater than C_T. As an illustration for $Ge(\eta = 1)$, at $I = 1.3$ mA, $g_m = 0.5$ mho and $C_D = 0.5\tau$. For $\tau = 20\mu s$, $C_D = 10\mu F$. The value of C_D is about a million times greater than the maximum value of C_T.

For Reverse Bias :

g_m is small, so that C_D is negligibly small in comparison with C_T

As $$C_D = \frac{\tau}{r} \quad \Rightarrow \quad C_D r = \tau \qquad ...(3.84)$$

Thus the diode time constant rC_D equals the mean life time of majority carriers and lies in the range of a few microsecond to hundreds of microseconds.

3.10 *PN*-Junction Diode Switching Characteristics

A junction diode may be used as a switch in electrical circuits. The circuit can be made ON or OFF by forward biasing or reverse biasing junction diode. In both the cases, the diode response is accompanied by a transient. The interval of time elapses before the diode recovers the steady state is called as *recovery time*. When the diode is switched from reverse-bias condition to forward bias condition, it takes certain time interval t_{fr}, called *forward recovery time*. This is defined as the time interval between the instant of 10% diode voltage to the instant, this voltage attains 90% of the final voltage. It is found that t_{fr} usually does not possess a serious practical problem and hence we have consider the more important situation of *reverse recovery time* t_{rr}.

Diode Reverse Recovery Time

Figure 3.21 shows the variation of steady state minority carrier density with distance x in a forward-biased *PN*-diode. The minority carrier holes in *N*-region are supplied from *P*-region while the minority carrier electrons in *P*-region are supplied from *N*-region. The concentration p_N of holes in *N*-region is increased above its thermal equilibrium value p_{N0}. Similarly, the concentration of n_P of electrons in *P*-region is increased above its thermal equilibrium value n_{P0}. The difference of excess holes *i.e.*, $(p_N - p_{N0})$ and excess of electrons *i.e.*, $(n_P - n_{P0})$ is shown in Fig. 3.21(*a*).

When the junction is reverse biased, the situation is shown in Fig. 3.21(*b*). As the minority carriers approach the junction, they are rapidly swept across, and the density of minority carriers diminishes to zero at this junction. The reverse saturation current I_0 is small because the density of thermally generated minority carriers is very small.

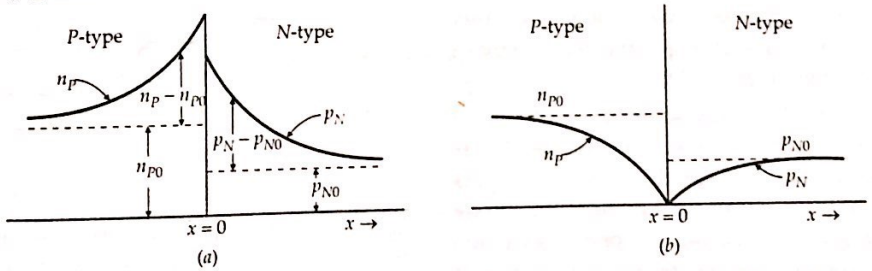


Figure 3.21 (*a*) Minority carrier density distribution as a function of distance x from the junction (forward bias)
(*b*) Minority carrier density distribution as a function of distance from the junction (reverse bias)

Let us consider the case when a diode carrying a current in the forward direction is suddenly reverse biased. By doing so, the diode current will not immediately fall to its steady state because the minority carrier distribution has to change to the steady state situation shown in Fig. 3.21(*b*) from that shown in Fig. 3.21(*a*). The diode will continue to conduct for a time, known as *diode reverse recovery time* t_{rr}, until excess minority carrier density $(p_N - p_{N0})$ or $(n_P - n_{P0})$ has dropped normally to zero. In this situation, the current is determined by the external resistance in the circuit.

Storage and Transition Time

Figure 3.22 shows the various events occurring in sequence on reverse biasing a conducting diode.

Let us consider that a time t_1 the input voltage v_i applied to a diode resistance circuit of Fig. 3.22(*a*) is reverse abruptly. Upto time t_1, the diode is conducting in the forward direction and voltage v_1 equals to forward voltage V_F. For large value of load resistance R_L, the voltage drop across R_L is large in comparison with the drop across the diode and hence the current flowing through R_L is given by $i \approx \left(\frac{V_F}{R_L}\right) = -I_R$ until the time $t = t_2$. At $t = t_2$, the injected minority carrier density at $x = 0$ has reached its equilibrium state as shown in Fig. 3.22(*c*). Now consider about the diode voltage v. At time t_1 the diode voltage falls slightly normally by $R_d(I_F + I_R)$ but does not reversed. Here R_d is the diode ohmic resistance. At time $t = t_2$, the process of sweeping of the excess minority carriers in the vicinity of junction back has completed. So the diode voltage begins to reverse and the diode current magnitude begins to reduce. During the time interval t_1 to t_2, the stored minority charge has remained stored and have this interval is called as storage time denoted by t_s. This is shown in Fig. 3.22(*e*).

After all excess minority carriers are swept out or recombined in the neighbourhood of the junction, the diode voltage begins to reverse. Now the magnitude of diode current begins to decrease exponentially to the normal steady state reverse saturation current

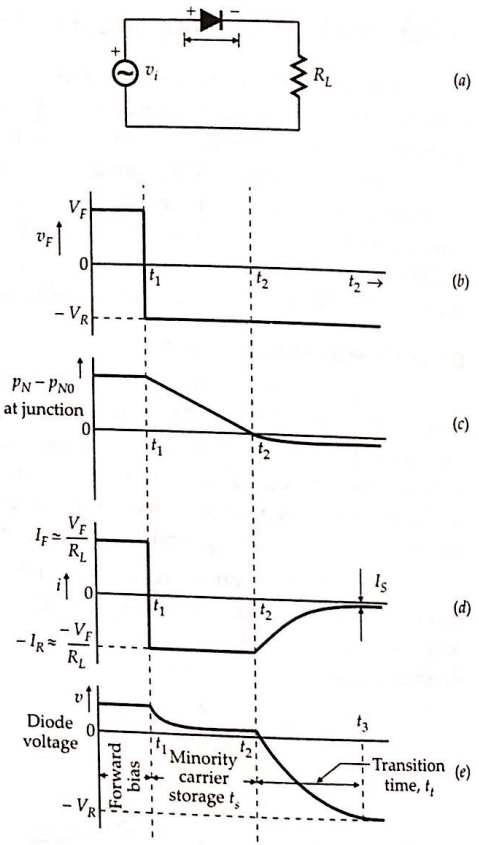


Figure 3.22 Waveform in a diode on reversing the : (*a*) circuit (*b*) applied voltage to the diode circuit (*c*) excess carrier density (*d*) diode current and (*e*) diode voltage.

value. The time interval between t_2 and the instant t_3 when the diode has recovered nominally, is called as transition time t_t. This recovery time interval is required for the minority carriers, which are at some distance from the junction, to diffuse the junction and cross it. In addition, the junction transition capacitance C_T across reverse-biased junction has charged through external resistor R_L to the voltage V_R.

For typical operating condition, manufacturers normally specify the reverse recovery time t_{rr} of a diode. It is the interval from the current reversal at $t = t_1$, until the diode has recovered to a specified extent either in terms of diode current or in terms of diode resistance. For commercial switching diodes, the reverse recovery time t_{rr} lies in the range from a low value of less than a nanosecond to such a large value as exceeding 1μs.

3.11 Piecewise Linear Diode Model

We know that the volt-ampere relationship is non-linear, it is difficult to analyse any circuit containing diodes. It may be easy with the help of piecewise linear approximation mode. For this approximation, we have to take any particular regions of operation of *VI*-characteristics, which are broken into linear segments and concept of a diode cut in voltage is also used.

The piecewise linear and continuous *VI*-characteristic is obtained on the inclusion of reverse resistance R_r in diode characteristics. Piecewise linear model is used when a more accurate model than ideal-diode model is needed but not restored to non-linear equation or graphical technique. The steps, which are used for piecewise linear diode model are given below :

(*i*) Approximation of actual *VI*-characteristics by straight line segment.

(*ii*) Model forward and reverse characteristics using a resistance in series with a constant voltage source.

A simple piecewise linear equivalent for diode is shown in Fig. 3.23.

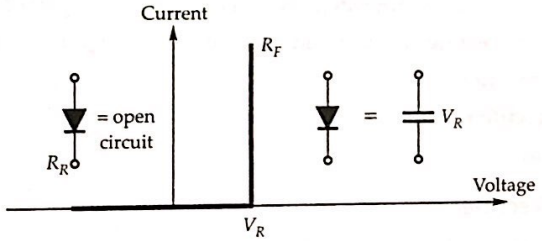


Figure 3.23 Characteristics piecewise linear diode.

It is well known that the diode is a binary device, at a given time, diode can exist only one of two possible states ON and OFF. If applied voltage exceeded the cut-in-voltage, V_R, the diode is forward biased and is said to be in ON state with diode forward resistance R_F. For a reverse bias, the diode is open circuited and is said to be in OFF state with infinitely large reverse resistance R_R.

This piecewise linear model is applied to analyse the diode circuits. Let us consider a circuit containing several diodes, resistors, power supplies. This type of circuit is analysed on the basis of state of diode. For ON state, the diode is replaced with R_F. Similarly, for OFF state, the diode is replaced with R_R. After replacing the diode with piecewise model, the entire circuit is linear.

Now we can make calculation using Kirchhoff's current and voltage laws (KCL and KVL). The assumption that a diode is ON, can be verified by the observation of sign of current through this diode. The assumption of diode is justified if the current is in forward direction. The assumption of diode is incorrect if the current is reverse direction. Under this condition, the analysis must begin with diode assumed to be OFF.

The diode OFF condition is tested by finding the voltage across it with trial and error method. If voltage is either in the reverse direction or in forward direction with a voltage less than V_R, the turn ON or cut-in voltage of diode, then the diode assumption is correct. However, if diode voltage is in the forward direction with a voltage greater than V_R, the condition of diode is ON and the original assumption is incorrect. Under this condition the analysis must being again with the diode assumed to be ON.

3.12 PN-Junction Diode as Rectifier

The process of converting ac voltage into dc voltage is known as *rectification*. DC power supplies are obtained with the help of :

(*i*) rectifier (*ii*) filter, and (*iii*) voltage regulator circuit

A device which converts ac voltage into dc voltage is called a rectifier.

Silicon diodes are generally used for power supply rectification. The non-linear characteristic of a diode is used to convert alternating current into unidirectional current. A rectifying diode can be considered as an ideal switch giving, zero forward resistance when forward biased and infinite resistance when reverse biased.

All rectifiers must provide a substantially one-way path for electric current. This is called unilateral conduction or a unidirectional conduction characteristic. Rectifier circuits employ one, two or four diode(s) to provide various degrees of rectifying effectiveness.

The following *three* rectifier circuits can be used :

- Half-wave rectifier,
- Full-wave rectifier, and
- Bridge rectifier

3.12.1 Half-wave Rectifier

The circuit diagram of a half-wave rectifier is shown in Fig. 3.24. It consists of a transformer, a diode and a load resistor. Depending on the output dc voltage required, a transformer of proper turns ratio $N_1 : N_2$ (step-up or step-down) is selected. The primary coil of a transformer is connected to the ac mains and the secondary coil to a load resistance R_L through the diode *D*. The voltage at the secondary coil of the transformer is the input for the rectifier.

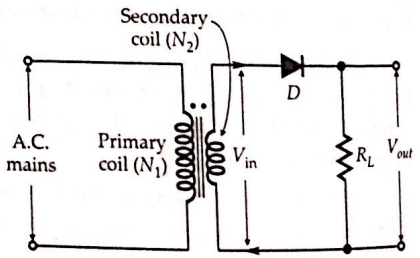


Figure 3.24 Half-wave rectifier.

at the secondary coil of the transformer.

- During the positive half-cycle of the input voltage, the diode D is forward biased and it conducts the current through R_L. Since the diode offers negligible resistance in the forward bias, the entire secondary voltage of transformer appears across R_L as output voltage.
- During the negative cycle (*i.e.*, the next half cycle) of the sine wave, the diode D is reverse biased. Hence no current flows in the circuit and no voltage develops across R_L.

Only the positive half cycle of the input appears across the load. The input ac voltage is converted in pulsating dc voltage as shown in Fig. 3.25. The process is known as *half-wave rectification*.

The output voltage is unidirectional, pulsating and intermittent. The output voltage contains a dc component and an ac component is known as ripple.

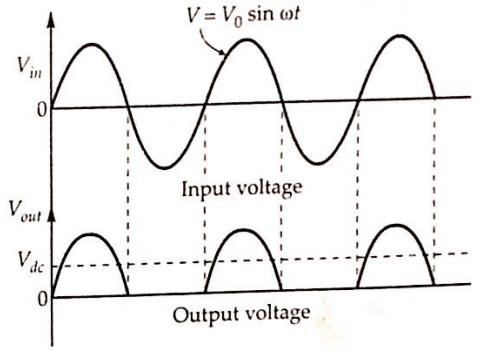


Figure 3.25 Input and output voltage waveform.

Analysis of Half-wave Rectifier Circuit

Performance Parameters

The performance of the half wave rectifier can be analysed by the following parameters :

(*i*) Peak inverse voltage (PIV).
(*ii*) Average values of output voltage and load current.
(*iii*) RMS value of load current.
(*iv*) Ripple factor (γ)
(*v*) Efficiency of rectification (η).
(*vi*) Voltage regulation.
(*vii*) Form factor.
(*viii*) Transformer utilization factor (TUF).

(*i*) ***Peak Inverse Voltage*** **(PIV).** During the negative half-cycle of the input, the diode is reverse biased. The voltage that appears across the load is nearly zero. All the input voltage now appears across the diode. The voltage across the diode is maximum when the input voltage is maximum. Thus the choice of diode should be such that the reverse breakdown voltage is greater than the input voltage.

The maximum reverse biased voltage that appears across the diode during the negative half cycle is called the *peak inverse voltage*.

Thus for a half wave rectifier

$$PIV = V_0 \qquad \text{...(3.85)}$$

(*ii*) ***Average values of Output Voltage and Load Current.*** Let $V = V_0 \sin \omega t = V_0 \sin \theta$ be the instantaneous sinusoidal voltage appearing at the secondary coil of a transformer.

If V_{dc} be the average or dc value of output voltage across R_L, then

$$V_{dc} = \frac{\text{Area under the curve over the full cycle}}{\text{Base}}$$

$$\Rightarrow \quad V_{dc} = \frac{\int_0^{\pi} V \, d\theta}{2\pi} = \frac{1}{2\pi} \int_0^{\pi} V_0 \sin \theta d\theta$$

$$\Rightarrow \quad V_{dc} = \frac{V_0}{2\pi} [-\cos \theta]_0^{\pi} = \frac{V_0}{2\pi} [1-(-1)]$$

$$\Rightarrow \quad V_{dc} = \frac{V_0}{\pi} = 0.318 \, V_0 \qquad \text{...(3.86)}$$

If I_{dc} is average value of load current, then

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_0}{\pi R_L} = \frac{I_0}{\pi} = 0.318 \, I_0 \qquad \text{...(3.87)}$$

where $I_0 = \dfrac{V_0}{R_L}$

Equations (3.86) and (3.87) show that average or dc value of load voltage or current is 31.8% of the maximum voltage or current.

Since the ac input voltage is applied through the transformer, it is necessary to include the secondary winding resistance R_S. The diode used is a practical diode and will have finite forward resistance.

Considering r_f is the average ac resistance of the diode, the peak value of load current will be

$$I_0 = \frac{V_0}{R_L + R_S + r_f} \qquad \text{...(3.88)}$$

Hence the dc load current

$$I_{dc} = 0.318 \, I_0 = 0.318 \frac{V_0}{R_L + R_S + r_f} \qquad \text{...(3.89)}$$

The load current I_L, which is composed of ac and dc components can be expressed using Fourier series is

$$I_L = I_0 \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{3\pi} \cos 2\omega t - \frac{2}{15} \cos 4\omega t + \ldots \right] \qquad \text{...(3.90)}$$

(*iii*) ***RMS value of Load current.*** The effective or *rms* value of load current is given by

$$I_{rms} = \sqrt{\frac{\int_0^{2\pi} I^2 d\theta}{2\pi}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_0^2 \sin^2\theta d\theta} \qquad [\because I = I_0 \sin\theta]$$

$$= \frac{I_0^2}{2\pi} \times \frac{1}{2}\left[\int_0^{\pi}(1-\cos 2\theta)d\theta + \int_0^{2\pi} 0.d\theta\right] = \sqrt{\frac{I_0^2}{4\pi}\left[\theta - \frac{\sin 2\theta}{2}\right]_0^{\pi}} = \sqrt{\frac{I_0^2}{4\pi}(\pi)} = \frac{I_0}{2}$$

i.e., $$I_{rms} = \frac{I_0}{2} = 0.5\, I_0 = 0.5\frac{V_0}{R_L} \qquad ...(3.91)$$

Thus $I_{rms} > I_{dc}$

(*iv*) ***Ripple Factor*** (γ). The output of half-wave rectifier is unidirectional, but fluctuates greatly with time. Hence, the output is a pulsating d.c. *i.e.* it contains dc and ac components. The undesired ac component is said to be *ripples*. How effectively a rectifier converts ac power into dc power is described quantitatively by terms such as ripple factor, rectification efficiency etc.

The ripple factor is a measure of purity of the dc output of a rectifier.

Ripple factor is defined as the ratio of the rms value of the ac component of load current to the average value of load current. It is a measure of imperfection in the dc output. The *rms* value of current is given by

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2}$$

$$\therefore \quad I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\therefore \quad \text{Ripple factor,} \quad \gamma = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}}$$

$$\gamma = \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_0/2}{I_0/\pi}\right)^2 - 1} \qquad [\because I_{rms} = I_0/2 \text{ and } I_{dc} = I_0/\pi]$$

$$= \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{(1.57)^2 - 1} = 1.21$$

$$\Rightarrow \quad \gamma = 1.21 \qquad ...(3.92)$$

Since $\gamma > 1$, it shows the rms value of ac component of wave (ripple) is greater than dc value of wave. Hence, the half-wave rectifier is a poor device for the conversion of ac voltage into dc voltage.

(v) ***Efficiency of Rectification*** (η). The efficiency of rectification is defined as the ratio of the dc output power to the input ac power.

$$\text{Rectifier efficiency } (\eta) = \frac{\text{Output dc power}}{\text{Input ac power}} = \frac{P_{dc}}{P_{ac}} \qquad \text{...(3.93)}$$

Now dc output power, $P_{dc} = I_{dc}^2 R_L = \frac{I_0^2}{\pi^2} R_L$

ac input power, $P_{ac} = I_{rms}^2 (R_S + R_L + r_f) = \frac{I_0}{2}(R_S + R_L + r_f) \qquad \left(\because I_{rms} = \frac{I_0}{2}\right)$

Efficiency $$\eta = \frac{I_0^2 R_L / \pi^2}{I_0^2 (R_S + R_L + r_f)/4}$$

or $$\eta = \frac{4R_L}{\pi^2 (R_S + R_L + r_f)} = \frac{0.406 R_L}{(R_S + r_f + R_L)} = \frac{0.406}{1 + \frac{(R_S + r_f)}{R_L}} \qquad \text{...(3.94)}$$

The efficiency will be maximum if $R_L >> (R_S + r_f)$

$$\eta_{max} = 0.406$$

$\therefore$ Maximum rectifier efficiency $\eta_{max} = 40.6\%$ ...(3.95)

This shows that in half-wave rectification, a maximum of 40.6% of ac power is converted into dc power. The ripple efficiency of the half-wave rectifier is the same as that of input because only one-half of each cycle of the ac input is used to produce dc output.

(*vi*) ***Voltage regulation.*** The regulation is a measure of the variation of the dc output as a function of the dc current and is defined as

$$\% \text{ Regulation} = \frac{V_{\text{no-load}} - V_{\text{full-load}}}{V_{\text{full-load}}} \times 100 \qquad \text{...(3.96)}$$

For an ideal power supply the % regulation will be zero. For a practical half-wave rectifier

$$\% \text{ Regulation} = \frac{R_S - r_f}{R_L} \times 100\%$$

$$\cong \frac{r_f}{R_L} \times 100\% \qquad [\text{when } R_S << r_f] \qquad \text{...(3.97)}$$

(*vii*) **Form Factor.** The form factor of the waveform is defined as the ratio of *rms* value of the load voltage to the dc component.

Form factor, $$F_p = \frac{V_{rms}}{V_{dc}} = \frac{I_{rms}}{I_{dc}} = \frac{I_0/2}{I_0/\pi} = \frac{\pi}{2} = 1.57 \qquad \text{...(3.98)}$$

Using the form factor, ripple factor $\gamma = \sqrt{F_p^2 - 1}$

(*viii*) ***Transformer Utilization Factor*** **(TUF).** In any power supply, the transformer rating is to be properly chosen. The factor which indicates how much is the utilization of the transformer in the circuit is called *transformer utilization factor.*

Transformer utilization factor with reference to the secondary is defined as the ratio of the dc power rating of the transformer secondary

$$TUF_s = \frac{\text{dc power delivered to the load}}{\text{ac power rating of the transformer secondary}}$$

For a half wave rectifier circuit

$$TUF_s = \frac{I_{dc}^2 R_L}{V_0 \frac{I_0}{2\sqrt{2}}} = \frac{\frac{I_0^2}{\pi^2} R_L}{\frac{V_0 I_0}{2\sqrt{2}}} = \frac{I_0 2\sqrt{2} R_L}{V_0 \pi^2}$$

$$\because \quad \frac{I_0}{V_0} = \frac{1}{R_L}, \quad TUF_s = \frac{2\sqrt{2}}{\pi^2} = 0.287 \qquad \text{...(3.99)}$$

It is clear that in half-wave rectifier circuit, the transformer is not fully utilized.

The TUF_p with reference to the primary has the same value of TUF_s.

Effect of Barrier Potential

When the practical diode model is used, the barrier potential of 0.7 V should be taken into account. During the positive half cycle, the input voltage must overcome the barrier potential, before the diode becomes forward biased. For a Si diode, this results in a half wave output with a peak value that is 0.7 V less than the peak value of the input. For Si, the expression for the output voltage is

$$V_{0(out)} = V_{0(in)} - 0.7\,\text{V} \qquad \text{...(3.100)}$$

This effect of the barrier potential is generally neglected when the peak value of the applied voltage is much greater than the barrier potential.

Disadvantages of Half-Wave Rectifier

There are some disadvantages or limitations of half-wave rectifier :

1. Since the ripple factor, $\gamma = 1.21$ is greater than dc value, the half wave rectifier is a poor device for the conversion of ac voltage into dc voltage.
2. Efficiency of rectification is very low ($\eta = 0.406$).
3. It has low *TUF i.e.,* 0.287.

Example 3.8 *A single phase half wave rectifier supplies power to a* 1 kΩ *load. If input supply voltage is* 200 *V rms and the forward resistance of diode is negligible, calculate :*

(*i*) *dc current in load* I_{dc} (*ii*) *dc voltage across load* V_{dc}

(*iii*) *ripple factor* γ (*iv*) *peak inverse voltage (PIV)*

Solution. Given $R_L = 1\,k\Omega = 1000\,\Omega$, $r_f << R_L$, $V_{rms} = 200\,V$

(*i*) In half wave rectifier $I_{dc} = \dfrac{I_0}{\pi} = \dfrac{V_0}{(R_L + r_f)\pi}$

$$\therefore \quad I_{dc} = \frac{V_0}{R_L \pi} = \frac{V_{rms}\sqrt{2}}{R_L \pi} = \frac{200\sqrt{2}}{1000 \times 3.14} = 90 \times 10^{-3}\,A = 90\,mA$$

(*ii*) DC voltage across load

$$V_{dc} = R_L I_{dc} = 1000 \times 90 \times 10^{-3} = 90\,V$$

(*iii*) Ripple factor

$$\gamma = \frac{I'_{rms}}{I'_{dc}} = \sqrt{\left[\frac{I^2_{rms}}{I^2_{dc}} - 1\right]} = \sqrt{\left(\frac{I_0/2}{I_0/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi^2}{2}\right)^2 - 1} = 1.21$$

(*iv*) $PIV = V_0 = V_{rms}\sqrt{2} = 200\sqrt{2} = 282\,V$

Example 3.9 *A half wave rectifier uses a transformer of turns ratio 8:1. If the primary voltage is 230 V(rms), find (i) d.c. output voltage, (ii) peak inverse voltage.*

Solution. Given $V_{rms} = 230\,V$

$\therefore$ Maximum primary voltage $= V_{rms}\sqrt{2}$

$$V_P = \sqrt{2} \times 230 = 324.3\,V$$

Since primary to secondary turn ratio $\dfrac{N_1}{N_2} = 8$

$\therefore$ Maximum secondary voltage

$$V_S = V_P \times \frac{N_2}{N_1} = 324.3 \times \frac{1}{8} = 40.54\,V$$

(*i*) d.c. output voltage

$$V_{dc} = I_{dc} \times R = \frac{I_0}{\pi} \times R = \frac{V_0}{\pi} = \frac{40.54}{3.14} = 12.9\,V$$

(*ii*) Since the diode is reverse biased, during negative half cycle of a.c. supply ; it conducts no current. Therefore, maximum transformer secondary voltage appears across the diode.

Hence peak inverse voltage, $PIV = V_S = 40.54\,V$

Example 3.10 *A half wave rectifier circuit shown in Fig. 3.24 has a load of 5 kΩ. Find the values (i) current in the circuit, (ii) dc output voltage across R_L, and (iii) voltage across the load. Given $V = 100 \sin 100\pi t$, $r_f = 20\,\Omega$.*

Solution. Given $V = 100 \sin 100\pi t$

Comparing the given equation with the standard equation

$V = V_0 \sin 2\pi\nu t$, we get

$V_0 = 100\,V$ and $\nu = 50\,Hz$

Since the diode conducts only during the positive half of the input voltage, we have

$$I_0 = \frac{V_0}{R_L + r_f} = \frac{100}{5000 + 20} = 20 \text{ mA}$$

Hence (*i*) Current $I = 20 \sin 100\pi t$ for $\pi < 100\pi t < 2\pi$

$= 0$ for $0 < 100\pi t < 2\pi$

(*ii*) d.c. output voltage

$$V_{dc} = I_{dc} \times R_L = \frac{I_0}{\pi} \times R_L = \frac{20 \times 10^{-3}}{3.142} \times 5 \times 10^3 = 31.5 \text{ V}$$

Output voltage $V_0 = 31.5 \sin 100\pi t$ for $\pi < 100\pi t < 2\pi$

$= 0$ for $\pi < 100\pi t < 2\pi$

(*iii*) Assuming the diode is an ideal diode, the voltage across it is zero during the forward biased. When the diode is reverse biased, the voltage across diode is

$V = 31.5 \sin 100\pi t$ for $0 < 100\pi t < \pi$

$= 0$ for $\pi < 100\pi t < 2\pi$

3.12.2 Full-Wave Rectifier

The circuit diagram of a full wave rectifier is shown in Fig. 3.26. It consists of two diodes D_1 and D_2 connected to the centre tapped secondary coil of transformer and a load resistor R_L. The primary coil of transformer is connected to the ac mains. Notice that only one-half of the total secondary voltage is used for each diode.

Let $V = V_0 \sin \omega t$ be the instantaneous sinusoidal voltage of frequency $\nu (= 50 \text{ Hz})$ appearing across the secondary coil. The secondary voltage is split into two halves, one half appearing across D_1 in series with R_L, the other half appearing across D_1 also in series with the load resistor, R_L.

During the positive half cycle of the ac input, the terminal A is positive with respect to B. The diode D_1 is forward biased.

The current therefore flows through the diode D_1 and voltage is developed across R_L. The direction of current is indicated by solid arrows.

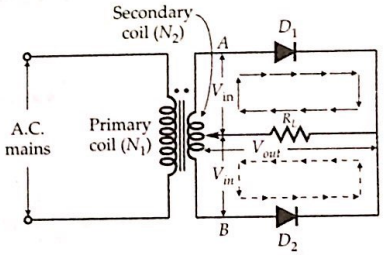


Figure 3.26 Full wave rectifier

During the negative half cycle, the terminal A is negative with respect to B. The diode D_2 is then forward biased. Consequently, the current flows through the load resistor R_L and is indicated by dotted arrows.

Note that the rectified current flows in the same direction through R_L during conduction in either diode. The diodes D_1 and D_2 conduct alternatively, and both halves of the input appear across load. Hence, the circuit functions as a full wave rectifier. The d.c. output voltage is positive at the common cathodes of the diodes.

The waveforms of the input ac voltage and output dc voltage are shown in Fig. 3.27.

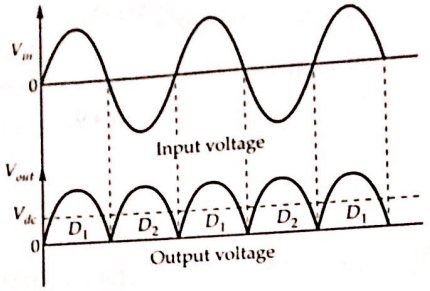


Figure 3.27 Input and output voltage waveform.

The rectified voltage is unidirectional, continuous but not constant.

(*i*) ***Peak Inverse Voltage*** **(PIV).** Each diode in a full-wave rectifier is alternatively forward biased and reverse biased. When the diode D_1 is forward biased, the voltage across the non-conducting diode D_2 is equal to the sum of the voltages across the lower half of the secondary coil and the load resistor *i.e.*, maximum diode voltage $V_{D2} = V_0 - (-V_0) = 2V_0$. Hence, peak inverse voltage across the non-conducting diode is given by

$$PIV = 2V_0 \qquad \text{...(3.101)}$$

(*ii*) ***Average value of output and Load current.*** Average or dc value of the output voltage

$$V_{dc} = \frac{\text{Area under the curve over a half cycle}}{\text{Base}}$$

$$= \frac{\int_0^{\pi} V d\theta}{\pi} = \frac{\int_0^{\pi} V_0 \sin\theta d\theta}{\pi} \qquad [\because V = V_0 \sin\theta]$$

$$= \frac{V_0}{\pi}\int_0^{\pi} \sin\theta\, d\theta = \frac{V_0}{\pi}[-\cos\theta]_0^{\pi} = \frac{V_0}{\pi}[1-(-1)]$$

$$\therefore \quad V_{dc} = \frac{2V_0}{\pi} = 0.636\, V_0 \qquad \text{...(3.102)}$$

The corresponding load current is given by

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_0}{\pi R_L} = 0.636\ I_0 \qquad \text{...(3.103)}$$

Equations (3.102) and (3.103) show that the average or dc value of load voltage or current is 63.6% of the maximum voltage or current.

Considering the secondary winding resistance R_S and the forward resistance r_f of the diode

$$I_{dc} = \frac{V_{dc}}{R_L + R_S + r_f} = \frac{2V_0}{\pi(R_L + R_S + r_f)}$$

Since two diodes conduct in alternate half cycles, the load current is given by

$$I_L = I_{D_1} + I_{D_2}$$

here $$I_{D_1} = I_0\left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t + \ldots\right]$$

and $$I_{D_2} = I_0\left[\frac{1}{\pi} - \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos\omega t - \frac{2}{15\pi}\cos 4\omega t - \ldots\right]$$

$\therefore$ $$I_L = I_0\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t\right]$$

(iii) ***RMS Value of Load Current.*** The *rms* value of load current is given by

$$I_{rms} = \sqrt{\frac{\int_0^{2\pi} I_L^2 d\theta}{2\pi}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_0^2 \sin^2\theta\, d\theta}$$

$$= \sqrt{\frac{I_0^2}{2\pi}\left[\int_0^{\pi}\sin^2\theta d\theta + \int_0^{2\pi}\sin^2\theta d\theta\right]} = \sqrt{\frac{I_0^2}{2\pi}\left(\frac{\pi}{2} + \frac{\pi}{2}\right)} = \frac{I_0}{2}$$

$$I_{rms} = \frac{I_0}{\sqrt{2}} = 0.707\, I_0 \qquad \ldots(3.104)$$

(iv) ***Ripple Factor*** **(γ).** The ripple factor for ful¹-wave rectifier is given by

$$\text{Ripple factor } (\gamma) = \frac{\text{RMS value of ac component}}{\text{dc component}}$$

Since the power dissipated in load resistance defines the *rms* value of current and total power is the sum of the power dissipated by the direct and alternating components, we have

$$I_{rms}^2 R_L = I_{dc}^2 R_L + I_{ac}^2 R_L$$

$$I_{ac}^2 = I_{rms}^2 - I_{dc}^2 \qquad \ldots(3.105)$$

and $$\text{Ripple factor } (\gamma) = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{I_0/\sqrt{2}}{2I_0/\pi} - 1} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = \sqrt{(1.11)^2 - 1}$$

$\therefore$ $$\gamma = 0.482 \qquad \ldots(3.106)$$

The lower ripple factor means that percentage of ac component in the output is smaller.

(*v*) ***Efficiency of Rectification.*** The rectifier efficiency is given by

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}} \qquad \text{...(3.107)}$$

Now, dc output power, $P_{dc} = I_{dc}^2 R_L = \left(\frac{2I_0}{\pi}\right)^2 R_L$

ac input power $P_{dc} = I_{rms}^2 (r_f + R_L + R_S) = \left(\frac{I_0}{\sqrt{2}}\right)^2 (r_f + R_L + R_S)$

$$\eta = \left(\frac{2I_0}{\pi}\right)^2 R_L \Big/ \left(\frac{I_0}{\sqrt{2}}\right)^2 (R_L + R_S + r_f)$$

$$= \frac{8}{\pi^2}\left[\frac{R_L}{R_L + R_S + r_f}\right] = 0.812\left[\frac{R_L}{R_L + R_S + r_f}\right]$$

The rectification efficiency is maximum if $R_L >> r_f + R_s$. Therefore, maximum efficiency $\eta_{max} = 81.2\%$.

Since the current repeats itself twice in every cycle of the supply voltage, the ripple frequency of the output voltage is twice ($2\nu = 100.8$ Hz) that of frequency of the input voltage.

(*vi*) ***Form Factor.*** It is given by, $F_P = \frac{I_{rms}}{I_{dc}} = \frac{I_0/\sqrt{2}}{2I_0/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$

(*vii*) ***Transformer Utilization Factor*** **(TUF).** Considering the secondary as made up of two half wave rectifiers feeding a common load resistor, the *TUF* with reference to the secondary is

$$TUF_s = \frac{\text{dc power to the load}}{\text{ac power rating of secondary}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{I_{dc}^2 R_L}{V_{rms} I_{rms}} = \frac{\left(\frac{2I_0}{\pi}\right) R_L}{\frac{V_0}{\sqrt{2}} \cdot \frac{I_0}{\sqrt{2}}} = \frac{8}{\pi^2}\frac{I_0 R_L}{V_0}$$

Since $V_0 = I_0 R_L$, $TUF_s = \frac{8}{\pi^2} = 0.812$

From the point of view of the primary, the dc current in the two halves of the secondary cancel. Hence, the TUF with reference to primary

$$TUF_P = 2 \times TUF \text{ of half wave} = 2 \times 0.287 = 0.574$$

Hence, average $TUF = \frac{TUF_P + TUF_S}{2} = \frac{0.574 + 0.812}{2} = 0.693$

Thus, in full-wave circuit, transformer gets utilized more than the half wave circuit.

...(3.107)

R_S)

maximum efficiency

voltage, the ripple
he input voltage.

as made up of two
the secondary is

f the secondary

circuit.

(*viii*) ***Voltage Regulation.*** Voltage regulation $= \dfrac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$

For a full-wave circuit

$$(V_{dc})_{NL} = \frac{2V_0}{\pi} = \frac{2I_0}{\pi}(R_L + R_S + r_f)$$

and $$(V_{dc})_{FL} = I_{dc}R_L = \frac{2I_0 R_L}{\pi}$$

$$\text{Voltage regulation} = \frac{\frac{2I_0}{\pi}(R_L + R_S + r_f) - \frac{2I_0}{\pi}R_L}{\frac{2I_0}{\pi}R_L}$$

$$\therefore \quad \text{V.R.} = \frac{R_S + r_f}{R_L} \quad \text{or} \quad \%\ \text{V.R.} = \frac{R_S + r_f}{R_L} \times 100$$

Advantage

The output voltage is continuous in comparison to half-wave rectifier.

Disadvantages

(*i*) It is difficult to locate the centre tap on the secondary winding.

(*ii*) The diode used must be of high PIV.

(*iii*) The dc output is small as each diode utilises only one-half of the transformer secondary voltage.

(*iv*) Transformer with centre tap is required.

Example 3.11 *A centre tapped full wave rectifier has a voltage of* $25\sin 314t$ *across each half of secondary winding. A load of* $1\,k\Omega$ *is connected in the circuit. Calculate : (i) peak value of current, (ii) d.c. value of current (Neglect resistance of diodes), (iii) RMS value of current, (iv) ripple factor (v) rectification efficiency and (vi) PIV of diode.*

Solution. Voltage across each half of secondary winding, $V = 25\sin 314t$, $V_0 = 25\,V$

(*i*) $I_0 = \dfrac{25}{1000} = 25\,mA$; (*ii*) $I_{dc} = \dfrac{2I_0}{\pi} = \dfrac{2\times 25}{\pi} = 15.9\,mA$

(*iii*) $I_{rms} = \dfrac{I_0}{\sqrt{2}} = \dfrac{25}{\sqrt{2}} = 17.67\,mA$

(*iv*) Ripple factor, $\gamma = \sqrt{\left(\dfrac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\dfrac{17.67}{15.9}\right)^2 - 1} = 0.482$

(*v*) Rectification efficiency $= \dfrac{P_{dc}}{P_{ac}} = \dfrac{I_{dc}^2 R_L}{I_{rms}^2 R_L} = \left(\dfrac{15.9}{17.67}\right)^2 = 81.2\%$

(*vi*) PIV of diode $= 2V_0 = 2\times 25 = 50\,V$.

Example 3.12 *A full wave rectifier circuit uses two diodes, each having a forward resistance r_f of* and infinite reverse resistance. The circuit is fed from a $200-0-200\ V_{rms}$ secondary winding of transformer. If the average current in the resistive load be 5A, calculate :

(a) the value of load resistance (b) PIV and (c) rectification efficiency

Solution. (a) Peak input voltage $V_0 = 200\sqrt{2}$.

If the forward resistance be r_f and load resistance be R_L, then peak current

$$I_0 = \frac{V_0}{(r_f + R_L)} = \frac{V_0}{R} = \frac{200\sqrt{2}}{R}$$

Average current $$I_{av} = \frac{2}{\pi} I_P = \frac{2}{\pi} \times \frac{200\sqrt{2}}{R}$$

$\therefore$ $$5 = \frac{400\sqrt{2}}{\pi R} \quad \text{or} \quad R = \frac{400\sqrt{2}}{5\pi} = 36\Omega$$

$\therefore$ $$r_f + R_L = 36\Omega \qquad \therefore \quad R_L = (36-6)\Omega = 30\Omega$$

(b) Peak inverse voltage of full wave rectifier $= 2V_0 = 400\sqrt{2}$

$\therefore$ PIV = 565.68 V

(c) Rectification efficiency

$$\eta = \frac{\text{dc output power delivered in load}}{\text{ac input power}}$$

Here dc output power $$= I_{dc}^2 R_L = \left(\frac{2}{\pi} I_0\right)^2 R_L = \left(\frac{400\sqrt{2}}{\pi R}\right)^2 R_L$$

AC input power $$= I_{rms}^2 R = \left(\frac{I_0}{\sqrt{2}}\right)^2 R$$

$\therefore$ $$\eta = \frac{\left(\frac{2}{\pi} I_0\right)^2 R_L}{\left(\frac{I_0}{\sqrt{2}}\right)^2 R} = \frac{\frac{4}{\pi^2} I_0^2 R_L}{\frac{I_0}{2}(r_f + R_L)} = \frac{8 R_L}{\pi^2 R} = \frac{8 \times 30}{\pi^2 \times 36} = \frac{20}{3\pi^2} = 67.54\%$$

Example 3.13 *Find the maximum dc voltage that can be obtained from the full-wave rectifier circuit.*

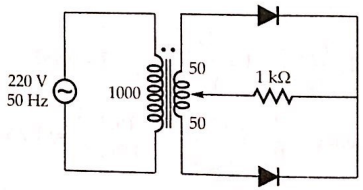


Figure 3.28

Solution. Given $V_0 = 220\,V$, $\nu = 50\,Hz$, $R_L = 1\,k\Omega$, $N_1 = 1000$, $N_2 = 100$

We know that $\frac{V_2}{V_1} = \frac{N_2}{N_1}$

RMS secondary voltage $V_2 = V_1 \times \frac{N_2}{N_1} = \frac{220 \times 100}{1000} = 22\,V$

Maximum secondary voltage, $V_{rms} = 22\sqrt{2} = 30.8\,V$

Maximum voltage across half-secondary winding $V_0 = \frac{30.8}{2} = 15.4\,V$

Average current $I_{dc} = \frac{2V_0}{\pi R_L} = \frac{2 \times 15.4}{3.14 \times 1000} = 9.89 \times 10^{-3}\,A$

DC output voltage $V_{dc} = I_{dc} \times R_L = 9.89 \times 10^{-3} \times 1 \times 10^2 = 9.89\,V$

3.12.3 The Bridge Rectifier

The bridge rectifier is the most frequently used circuit for electronic dc power supplies. It does not need a centre tap transformer. In the case of a full-wave rectifier using a centre-tap transformer, the centre-tap may not provide an exact centre-tap and hence, two input half wave may not be of equal size. Hence, the adjacent pulses in the output waveform will be of unequal size. This is eliminated in bridge rectifier using four diodes.

The circuit diagram of a bridge rectifier is shown in Fig. 3.29. It consists of four diodes D_1, D_2, D_3 and D_4 connected in the form of a bridge *ABCD*. Two leads *A* and *C* of the network are connected to the secondary coil and the other two leads *D* and *B* connected to the load resistance R_L.

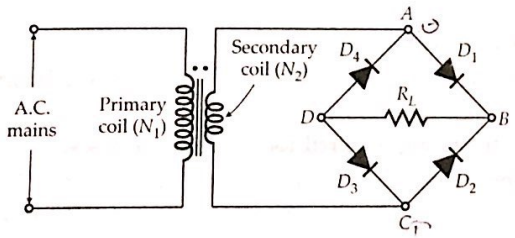


Figure 3.29 Bridge rectifier

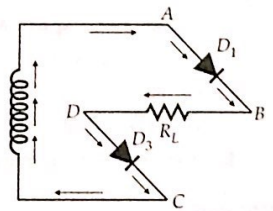


Figure 3.30 Bridge rectifier during positive half cycle.

Let $V = V_0 \sin\theta$ be the instantaneous sinusoidal voltage of frequency, $\nu (= 50\,Hz)$ appearing across the secondary coil of transformer.

During the positive half cycle, the circuit terminal *A* is positive with respect to C. The diodes D_1 and D_3 are forward biased and act as short circuit. At this instant, the diodes D_2 and D_4 are reverse biased and hence act as open circuit. The current flows in the direction $AD_1BR_LDD_3CA$ producing a voltage drop R_L as shown in Fig. 3.30.

During the negative half cycle the terminal A is negative with respect to C. The diodes D_2 and D_4 are forward biased and diodes D_1 and D_3 are reverse biased. The current flows along $CD_2BR_LDD_4AC$ producing a voltage drop across R_L as shown in Fig. 3.31.

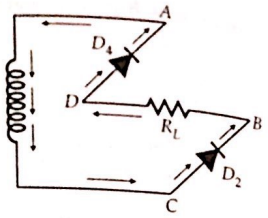


Figure 3.31 Bridge rectifier during negative half cycle.

Thus, there is output voltage during both halves of the input cycle. The rectifier is therefore, a full-wave rectifier. The input voltage and output voltage waveforms are same as that of full-wave rectifier as shown in Fig. 3.26.

The output voltage is unidirectional continuous but not constant.

The output dc voltage and current, the rms current, ripple factor and efficiency will be the same as for a centre tapped rectifier.

The frequency of output voltage is twice that of the frequency of input voltage.

i.e.,

$$v_0 = 2v_i \qquad \text{...(3.108)}$$

Peak Inverse Voltage (PIV)

During the positive half cycle of input signal, the diodes D_1 and D_3 are conducting. Neglecting the forward resistance of the diodes, the entire input peak voltage appears across the load R_L. At this instant, the diodes D_2 and D_4 are reverse biased. Hence, the voltage across the non-conducting D_2 and D_4 is also V_0. Thus,

$$\text{PIV} = V_0 \qquad \text{...(3.109)}$$

Advantages

1. It does not require a transformer with centre tapped secondary.
2. The output voltage is twice that of centre tapped rectifier for the same secondary voltage.
3. The PIV rating need be only half the rating required for full wave rectifier.
4. It is suitable for light voltage applications.

Disadvantages

1. It uses four diodes.
2. Since two diodes in series are always carrying current, the voltage drop and power loss in diodes in the bridge circuit is more than that in the full-wave circuit. This factor assumes greater importance in high voltage circuits.

NOTE *Now-a-days, the bridge rectifiers are so common that manufacturers are packing them as a single unit with bakelite or some other plastic encapsulation with external connections brought out.*

Example 3.14 *In a bridge rectifier circuit the peak value of secondary voltage is $240\sqrt{2}$ V and frequency is 50 Hz. Determine no load dc voltage, PIV and output frequency.* **[GGSIPU, Nov. 2013 (2-5 marks)]**

Solution. Given $V_0 = 240\sqrt{2}$ V, $\nu = 50$ Hz

(*i*) dc output voltage $V_{dc} = \dfrac{2V_0}{\pi} = 216.15$ V (*ii*) $PIV = 2V_0 = 2 \times 240 \times \sqrt{2}$ V $= 678.72$ V

(*iii*) $f_{out} = 2f_{in} = 2 \times 50$ Hz $= 100$ Hz

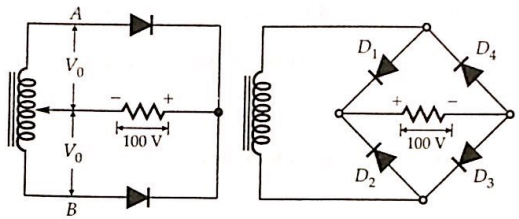
Example 3.15 *If the output voltage of a centre tap full-wave rectifier and a bridge type full-wave rectifier is 100 V, determine the peak inverse voltage in both cases. Comment upon the results.*

Solution. The two rectifier circuits are shown in Fig. 3.32.

(*i*) Centre tap full-wave rectifier circuit is shown in Fig. 3.32(*a*). Maximum value of voltage between centre tap and each side of the secondary,

$$V_0 = \frac{\pi V_{dc}}{2} = \frac{\pi \times 100}{2} = 157.08 \text{ V}$$

$$\left[\because V_{dc} = V_{av} = \frac{2V_0}{\pi}\right]$$



(*a*) Center tap circuit (*b*) Bridge circuit

Figure 3.32

Peak inverse voltage coming across each diode

$$PIV = 2V_0 = 2 \times 157.08 = 314.16 \text{ V}$$

(*ii*) Bridge-type full-wave rectifier circuit is shown in Fig. 3.32(*b*).

Maximum value of voltage across the secondary,

$$V_0 = \frac{\pi V_{dc}}{2} = \frac{\pi \times 100}{2} = 157.08 \text{ V}$$

Peak inverse voltage coming across each diode

$$PIV = V_0 = 157.08 \text{ V}$$

Comments. The above results show for same dc output voltage, PIV in case of bridge circuit is half to that of centre tap rectifier circuit. Therefore, crystal diode of higher (double) peak inverse voltage are required for centre-tap full-wave rectifier circuit. This is a distinct advantage of bridge circuit.

Example 3.16 *In the bridge type circuit shown in Fig. 3.33, the diodes are considered to be ideal.*

Calculate

(*i*) *dc output voltage,* (*ii*) *PIV,*

(*iii*) *rectification efficiency, and*

(*iv*) *output frequency.*

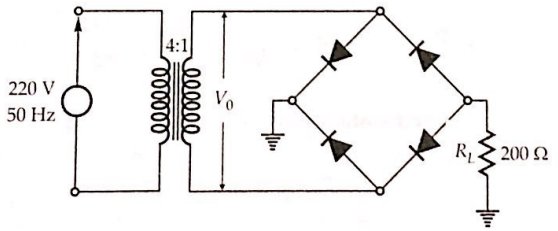


Figure 3.33

Solution. (*i*) Here primary to secondary turn ratio $\frac{N_1}{N_2} = 4$

$\therefore$ RMS primary voltage $= 220$ V

$\therefore$ RMS secondary voltage $= 220 \times \frac{1}{4} = 55$ V

Peak voltage at the secondary $= V_0 = 55\sqrt{2} = 77.79$ V

Average current, $I_{dc} = \frac{2}{\pi} I_0 = \frac{2}{\pi} \frac{V_0}{R_L} = \frac{2 \times 77.79}{\pi \times 200} = 0.2476$ A

DC output voltage, $V_{dc} = I_{dc} \times R_L = 0.2476 \times 200 = 49.52$ V

(*ii*) The peak inverse voltage = maximum secondary voltage = 77.79 V

(*iii*) Rectification efficiency, $\eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{2I_0}{\pi}\right)^2 R_L}{\left(\frac{I_0}{\sqrt{2}}\right)^2 R_L} = 82.1\%$

(*iv*) Output frequency is twice that ac supply frequency

$\therefore \quad \nu_{out} = 2\nu_{in} = 2 \times 50 = 100$ Hz

Example 3.17 *Output of a transformer used in a bridge rectifier is* $25 \sin 314\,t$. *A load of* $1\,k\Omega$ *is connected in the circuit. Calculate : (i) peak value of current ; (ii) dc value of current ; (iii) rms value of current, (iv) ripple factor, (v) rectification efficiency and (vi) PIV of diode. Neglect resistance of diodes.*

Solution. $V = 25 \sin 314t$, $V_0 = 25$, then

(*i*) $I_0 = \frac{25}{1000} = 25$ mA

(*ii*) $I_{dc} = \frac{2I_0}{\pi} = \frac{2 \times 25}{3.14} = 15.9$ mA

(*iii*) $I_{rms} = \frac{I_0}{\sqrt{2}} = \frac{25}{1.414} = 17.67$ mA

(*iv*) Ripple factor, $\gamma = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\left(\frac{7.67}{15.9}\right)^2 - 1} = 0.482$

(*v*) Rectification efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{I_{dc}^2 R_L}{I_{rms}^2 R_L} \times 100 = \left(\frac{15.9}{17.67}\right)^2 \times 100 = 81.2\%$$

(*vi*) PIV of diode $= V_0 = 25$ V

3.12.4

3.12.4 Comparison of Practical Rectifier Circuits

S.No.	Performance measure	Half-wave	Full-wave	Bridge
1.	Number of diodes	1	2	4
2.	Transformer necessary	No	Yes	Yes
3.	Secondary line-to-line voltage	$V_0 / \sqrt{2}$	$2V_0 / \sqrt{2}$	$V_0 / \sqrt{2}$
4.	PIV	V_0	$2V_0$	V_0
5.	DC voltages	V_0 / π	$2V_0 / \pi$	$2V_0 / \pi$
6.	RMS current	$I_0 / 2$	$I_0 / 2$	$I_0 / \sqrt{2}$
7.	Ripple factor (γ)	1.21	0.482	0.482
8.	Efficiency of rectification (η)	40.6	81.2	81.2
9.	Ripple frequency	ν_i	$2\nu_i$	$2\nu_i$

3.13 Diode Clippers

The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave to suit a particular device is called a *clipping circuit* or *clipper*. Clipping circuits are widely used in RADAR, digital and other electronic systems. Although several clipping circuits have been developed to change the waveform, but here we shall consider only the diode clipping circuits.

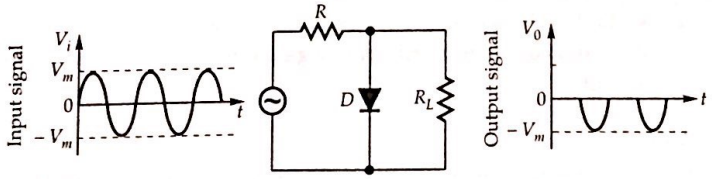
A clipping circuit usually consists of a diode and a resistor. Sometimes a dc battery is also used to fix the clipping level. A clipping circuit can remove signal voltages above and below a specified level.

Important clipping circuits or clippers are :

- positive clipper
- negative clipper
- biased clipper
- combination clipper

3.13.1 Positive Clipper

A positive clipper is one which removes (or clipps off) the positive half cycles of the input voltage. Figure 3.34 represents a typical circuit of a positive circuit or a positive clipper using a diode along with input and output voltages.



(*a*) Input voltage (*b*) Circuit diagram (*c*) Output voltage

Figure 3.34 Positive clipper

Action of Circuit

During the positive half cycle of input ac signal, the diode is forward biased and conducts heavily. Therefore the diode acts as short circuit and the voltage across it is zero and hence the voltage across the load R_L is also zero *i.e.*, the output voltage during positive half cycle is zero.

During the negative half cycle of input voltage, the diode is reverse biased and behaves as an open circuit. In this case the circuit behaves as potential divider with an output V_0 given by

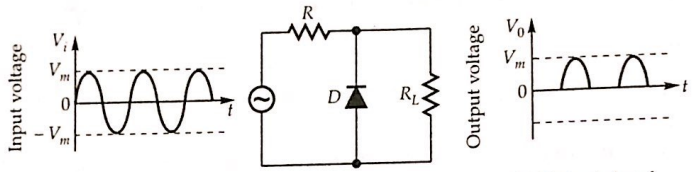
$$V_0 = \frac{R_L}{R + R_L} V_i \qquad ...(3.110)$$

Generally, $R_L >> R$, and $V_0 = V_i$

Thereby indicating that the negative cycle is present as such. Thus output voltage has all positive cycles removed or clipped off.

3.13.2 Negative Clipper

A negative clipper is one which removes all the negative cycles of the input voltage. Figure 3.35 represents the typical circuit of a negative clipper using a diode along with input and output voltages.



(*a*) Input signal (*b*) Circuit diagram (*c*) Output signal

Figure 3.35 Negative clipper

Circuit Action

During the positive half cycle of input ac signal the diode is reverse biased and acts as an open circuit.

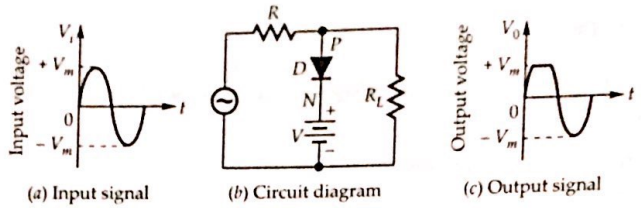
In this case the circuit behaves as a potential divider with output voltage V_0 given by

$$V_0 = \frac{R_L}{R + R_L} \qquad ...(3.111)$$

Generally $V_D \approx V_i$ (as $R_L >> R$). Thus the positive half cycle is presented as such. During the negative half cycle, the diode is forward biased and act as a *short circuit* and hence voltage across R_L is zero, *i.e.*, output is zero. In other words, the negative half cycles of input are removed or clipped off from the output.

3.13.3 Biased Clipper

A biased clipper is one which removes a small portion of the positive or negative half cycle of the signal voltage. Figure 3.36 represents the circuit diagram of a biased positive clipper using a diode, a resistor R and a battery of V volts along with input and output voltages.



(a) Input signal (b) Circuit diagram (c) Output signal

Figure 3.36 Biased clipper

Circuit Action

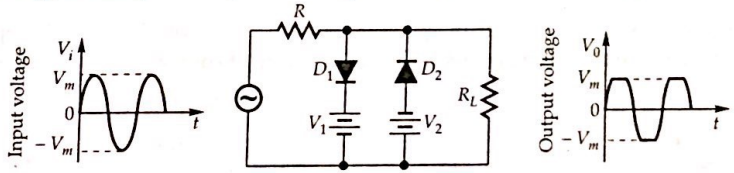
During positive half cycle the diode is forward biased if the input voltage exceeds the battery voltage +V. Under this condition the diode acts as a short circuit and the output voltage remains equal to +V. But if the input voltage is less than +V, the diode is reverse biased and acts as an open circuit. Therefore, the most of input voltage appears across the output. In this way the biased positive clipper removes the input voltage above +V.

During the negative half cycle of input voltage, the diode is reverse biased. Therefore almost entire negative half cycle appears across the load.

If it is desired to remove the portion of negative half cycle, the polarities of diodes or batteries are reversed. Such a circuit is then called biased negative clipper.

3.13.4 Combination Clipper

A combination clipper is a combination of biased positive and negative clippers and removes a portion of both positive and negative half cycle of input voltages. The current of combination clipper along with input and output voltages is shown in Fig. 3.37.



(a) Input signal (b) Circuit diagram (c) Output signal

Figure 3.37 Combination clipper

Circuit Action

During positive half cycle, when positive input voltage is greater than $+V_1$, the diode D_1 is forward biased and acts as short and diode D_2 being reverse biased is open. Therefore, a voltage $+V_1$ appears across the load. During negative half cycle if input voltage is greater than $-V_2$, the diode D_2 is forward biased and acts as a short while diode D_1 is reverse biased and acts as open. Therefore the output voltage remains $-V_2$.

When the input voltage is between $+V_1$ and $-V_2$ neither diode is forward biased, therefore in this condition most of the input voltage appears across the load R_L.

NOTE *This clipping circuit can give square wave output if maximum value of input voltgage is much greater than clipping levels.*

3.14 Diode Clamper

A circuit that introduces a dc level into an ac signal is called the clamping circuit or a clamper.

Figure 3.38 represents the concept of clamping.

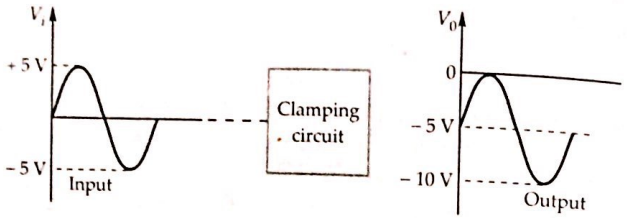


Figure 3.38 Concepts of clamping.

The input signal is a sine wave of peak value +5 V at 0 V dc level. The clamping circuit adds dc level −5 V to ac signal. Therefore positive peak falls from +5 V to 0 V and negative peak falls from −5 V to −10 V. The clamping circuit does not change the shape of original signal but only the dc level of ac signal is shifted.

Zero Level Clamping Circuit

(*i*) Positive Peak Clamper or Negative dc Restoring Circuit

The positive peak clamper shifts the positive peak to zero level. Figure 3.39 represents the circuit along with input and output signals. The clamping circuit consists of diodes, a capacitor and a load resistance.

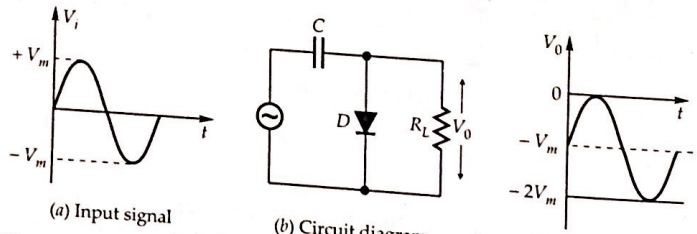


Figure 3.39 Positive peak clipper

Circuit Action

Let us assume the diode as ideal one and the value of R_L and C are chosen such that $R_L C$ has large value. Initially the capacitor is uncharged and has no voltage across it.

During positive half cycle input signal, positive diode is forward biased and acts as a short circuit as shown in Fig. 3.40.

The capacitor C charges through diode D and the input voltage source. Assuming diode as an ideal one, the potential drop across diode is zero and the potential drop across capacitor $\cong V_m$.

The capacitor C maintains a constant voltage across it due to large time constant $R_L C$. In the steady state, the capacitor acts as a constant voltage source of V_m volts. In the steady state the output voltage can be expressed as

$$V_0 = V_i - V_m \qquad ...(3.112)$$

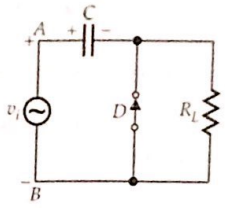


Figure 3.40 Positive half cycle.

If $V_i = V_m \sin \omega t$, then $V_0 = V_m \sin \omega t - V_m$ and at $t = \frac{T}{4}, \frac{5T}{4}, \ldots, V_0 = V_m - V_m = 0$ V *i.e.*, positive peak is clamped to zero volt and the positive half cycle in output lies between $-V_m$ to 0 V.

During negative half-cycle, the diode is reverse biased and acts as a *open circuit* as shown in Fig. 3.41. The output voltage is now

$$V_0 = V_i - V_m = -V_m \sin \omega t - V_m$$

and at $t = \frac{3T}{4}, \frac{7T}{4}, \ldots, V_0 = -2\, V_m$.

Clearly, this circuit introduces a dc level $-V_m$ to ac signal and positive peak is clamped at 0 V. That is why the circuit is called positive peak clamping circuit or negative dc restoring circuit.

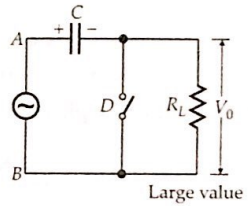
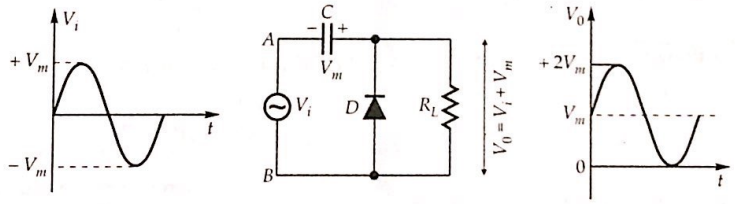


Figure 3.41 Negative half cycle.

(*ii*) Negative Peak Clamping Circuit or Positive dc Restoring Circuit

The circuit along with input and output signal is shown in Fig. 3.42.



(*a*) Input signal (*b*) Circuit diagram (*c*) Output signal

Figure 3.42 Negative Peak Clamping

The circuit action is as for positive peak clamping circuit except that the polarities of capacitor are reversed. Since in this case the diode is forward biased and acts as a short circuit during negative half cycle.

The output voltage is $V_0 = V_i + V_m$ *i.e.*, dc level of $+V_m$ is introduced in ac level and negative peak is shifted to zero volt.

3.6 DC resistance/static resistance

$$R_{dc} = \frac{V_F}{I_F}$$

3.7 AC resistance/dynamic resistance

$$R_{ac} = \frac{\Delta V_F}{\Delta I_F}$$

3.8 Average AC resistance

$$R_{av} = \frac{\Delta V_F}{\Delta I_F}$$

3.9 Space charge capacitance

$$C_T = \left| \frac{dQ}{dV} \right|$$

where dQ = increase in charge, and

dV = increase in voltage

(*i*) for step graded junction

$$C_T = \frac{\varepsilon A}{W}$$

A = Area and W = plate separation

(*ii*) Linearly C_{T_d} +

and current density is given

$$I = I_0 \exp\left[\frac{eV}{k_B T} - 1\right]$$

or $$\exp\left[\frac{eV}{k_B T} - 1\right] = \frac{I}{I_0} = 4 \times 10^5 \quad \text{or} \quad \frac{eV}{k_B T} \approx \ln 4 \times 10^5 = 12.9$$

Then $$V = \frac{12.9 \times k_B T}{e} = \frac{12.9 \times 138 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} = 0.33 \text{ V}$$

Problem 3.2 *An alloyed junction is forward by melting a pellet of* I_N *to an N-type Si of conductivity* $200 W^{-1} m^{-1}$. *If the conductivity of the alloyed region is* $3.6 \times 10^4 W^{-1} m^{-1}$ *and intrinsic concentration of Si is* $1.5 \times 10^{16}/m^3$, *determine the constant potential at 27° C. The mobilities of electrons and holes are 0.135 and* $0.048 m^2/Vs$ *respectively.*

Solution. Given $\sigma_N = 200 \text{ W}^{-1}\text{m}^{-1}$, $\sigma_P = 3.5 \text{ W}^{-1}\text{m}^{-1}$, $n_i = 1.5 \times 10^6/\text{m}^3$, $\mu_N = 0.135 \text{ m}^2/\text{Vs}$ and $\mu_P = 0.048 \text{ m}^2/\text{Vs}$

For the *N*-type Si, we have

$$\sigma_N = en\mu_N = eN_D\mu_N$$

∴ Donor concentration $$N_D = \frac{\sigma_N}{e\mu_N} = \frac{200}{1.6 \times 10^{-19} \times 0.135} = 9.26 \times 10^{21} \text{ m}^3$$

Similarly, the acceptor concentration in the *P*-region is

$$N_A = \frac{\sigma_P}{e\mu_P} = \frac{3.6 \times 10^4}{1.6 \times 10^{-19} \times 0.048} = 4.69 \times 10^{24}/\text{m}^3$$

Contact potential $$V_B = \frac{k_B T}{e} \ln \frac{N_D N_A}{n_i^2}$$

$$= 0.026 \ln \frac{(9.26 \times 10^{21})(4.69 \times 10^{24})}{(1.5 \times 10^{16})^2} = 0.86 \text{ V}$$

Problem 3.3 *The current flowing in a certain PN-junction at room temperature is* 2×10^{-7} *A, when a large reverse bias voltage is applied. Calculate the current flowing 0.1 V is applied.*

Solt tion. Given $I_0 = 2 \times 10^{-7}$ A, $V = 0.1$ V

The volt-ampere relation for a junction diode is given by

$$I = I_0(e^{eV/k_B T} - 1) = (2 \times 10^{-7}) \times [e^{V/0.026} - 1]$$

$$= (2 \times 10^{-7}) \times [e^{0.1/0.026} - 1] = 91.62 \times 10^{-7} = 9.16 \text{ μA}$$

Problem 3.4 *A silicon diode has a saturation current of 0.1 pA at 20° C. Find its current when it is forward biased at 0.55 V. Find the current in the same diode when the temperature rises to 100° C.*

Solution. $\eta = 2$, $I_0 = 0.1 \text{ pA} = 1.0 \times 10^{-13}$ A, $V = 0.55$ V

Then from diode equation

$$I = I_0\left[\exp.\frac{V.e}{\eta k_B T} - 1\right]$$

$$= 0.1 \times 10^{-12}\left[\exp.\frac{0.55 \times 1.6 \times 10^{-19}}{2 \times 1.38 \times 10^{-23} \times 293}\right]$$

$$= 1.0 \times 10^{-13}\left[\exp.\frac{0.55}{2 \times 0.026} - 1\right]$$

$$= 1.0 \times 10^{-13} \times 54867.7 = 5.49 \times 10^{-9} \text{ A} = 5.49 \text{ nA}$$

When the temperature rises to 100° C

Then $$V_T = \frac{1.38 \times 10^{-23} \times 373}{1.6 \times 10^{-19}} = 0.0322 \text{ V}$$

Then $$I' = 1.0 \times 10^{-13}[e^{\frac{0.55}{2 \times 0.0322}} - 1] = 1.0 \times 10^{-13}[5116.2] = 0.51 \text{ nA}.$$

Problem 3.5 *A PN-junction is formed from germanium of conductivity* $0.8 \Omega^{-1} cm^{-1}$ *on the P-side and* $1.6 \Omega^{-1} m^{-1}$ *on the N-side. Calculate potential barrier and the depletion layer at 300 K* ($n_i = 2.1 \times 10^{13}/cm^3$) $\mu_P = 2000 cm^2/Vs$ *and* $\mu_N = 4000 cm^2/Vs$. *The relative dielectric constant for germanium is 16 and the Boltzman constant* $k_B = 1.38 \times 10^{16} erg/K$.

Solution. given $\sigma_N = 1.6 \times \Omega^{-1}\text{cm}^{-1}$, $\sigma_P = 0.8\Omega^{-1}\text{cm}^{-1}$, $\varepsilon_r = 16$, $\mu_P = 2000 \text{ cm}^2/\text{Vs}$, $\mu_N = 4000 \text{ cm}^2/\text{Vs}$, $k_B = 1.38 \times 10^{-16} \text{ erg/K}$, $n_i = 2.1 \times 10^{13}/\text{m}^3$.

Taking the majority carriers contributing mainly to the conductivity, we can write

$$N_D = \frac{\sigma_N}{e\mu_N} = \frac{1.6}{(1.6 \times 10^{-19}) \times 4000} = 2.5 \times 10^{15}/\text{cm}^3$$

$$N_A = \frac{\sigma_P}{e\mu_P} = \frac{0.8}{(1.6 \times 10^{-19}) \times (2000)} = 2.5 \times 10^{15}/\text{cm}^3$$

At 300 K

$$\frac{k_B T}{e} = \frac{(1.38 \times 10^{-16}) \times 300 \times 10^7}{(1.6 \times 10^{-19})} = 0.0258 \text{ V}$$

Both sides have been multiplied by 10^7 to convert ergs into joules.

The barrier potential is

$$V_B = \frac{k_B T}{e} \log\left(\frac{N_D N_A}{n_i^2}\right)$$

$$= 0.0258 \log\left[\frac{6.25 \times 10^{30}}{4.41 \times 10^{26}}\right] = 0.2467 \text{ V}$$

The width of depletion layer is

$$x = \left[\frac{2\varepsilon V_B}{e(N_A + N_D)^{1/2}}\right]^{1/2} \times \left[\left(\frac{N_D}{N_A}\right)^{1/2} + \left(\frac{N_A}{N_D}\right)^{1/2}\right]$$

Here $\frac{N_D}{N_A} = \frac{N_A}{N_D} = 1$ and $N_A + N_D = 5 \times 10^5$, $\varepsilon_r = 16$

$$x = \left[\frac{2 \times 16 \times (8.854 \times 10^{-14}) \times 0.2467}{(1.6 \times 10^{-19}) \times (5 \times 10^{15})}\right]^{1/2} [(1)^{1/2} + (1)^{1/2}] = 1.9 \times 10^{-4} \text{ cm}$$

Problem 3.6 *A half wave rectifier is used to supply 50 V dc to a resistive load of 800 Ω. The diode has a resistance 25 Ω. Calculate ac voltage required.*

Solution. Given : $V_{dc} = 50$ V, $r_f = 25\Omega$, $R_L = 800\Omega$

Let V_0 be the maximum value of a.c. voltage required

$$\therefore \quad V_{dc} = I_{dc} \times R_L = \frac{I_0}{\pi} \times R_L = \frac{V_0}{\pi(r_f + R_L)} \times R_L \qquad \left[\text{Here } I_0 = \frac{V_m}{r_f + R_L}\right]$$

or $$50 = \frac{V_0}{\pi(25 + 800)} \times 800$$

$$\therefore \quad V_0 = \frac{\pi \times 825 \times 50}{800} = 162 \text{ V}.$$

Problem 3.7 *A full wave rectifier uses two diodes, the internal resistance of each diode may be assumed constant at 20 Ω. The transformer rms secondary voltage from centre tap to each end of secondary is 50 V and load resistance is 980 Ω. Find : (i) the mean load current and (ii) the rms value of load current.*

Solution. Given $r_f = 20\Omega$, $R_L = 980\Omega$, $V_{rms} = 50$ V

Maximum ac voltage $V_0 = 50\sqrt{2} = 70.7$ V

Maximum load current $I_0 = \frac{V_m}{r_f + R_L} = \frac{70.7 \text{ V}}{(20 + 980)\ \Omega} = 70.7$ mA

(*i*) Mean load current $I_{dc} = \frac{2I_0}{\pi} = \frac{2 \times 70.7}{\pi} = 45$ mA

(*ii*) RMS value of load current is $I_{rms} = \frac{I_0}{\sqrt{2}} = \frac{70.7}{\sqrt{2}} = 50$ mA

Problem 3.8 *An ideal germanium diode has a reverse saturation current of 30 μA at a temperature of 125° C. Find the dynamic resistance at that temperature for 0.2 V bias in (a) forward direction and (b) the reverse direction.*

Solution. Given : $T = 125° C = 398$ K, $I_0 = 30\mu$A, $V_F = 0.2$ V and $\eta = 1$.

(*a*) Dynamic resistance in forward direction

$$V_T = \frac{T}{11600} = \frac{398}{11600} = 0.0343 \text{ V}$$

$\therefore$ Diode current equation, $I = I_0[e^{V_F/\eta V_T} - 1]$

Differentiating the above equation with respect to V

$$\frac{dI}{dV} = \frac{I_0}{V_T} e^{V_F/V_T}$$

or $$\frac{1}{R_{ac}} = \frac{I_0}{V_T} e^{V_F/V_T} \qquad \left[\because R_{ac} = \frac{dV}{dI}\right]$$

or $$R_{ac} = \frac{V_T}{I_0} e^{-V_F/V_T} = \frac{0.343}{30 \times 10^{-6}} e^{-0.2/.0343} = 3.36\ \Omega$$

(*b*) Dynamic resistance in reverse direction

$$R_{ac} = \frac{V_T}{I_0} e^{+V_F/V_T} = \frac{0.0343}{30 \times 10^{-6}} e^{+0.2/0.0343} = 0.389\ \text{M}\Omega$$

Problem 3.9 *Consider the circuit shown in Fig. 3.43. A string of three diodes is used to provide a constant voltage of 2.1 V. Calculate percentage change in this regulated voltage caused by*

(*a*) *± 10% change in power supply.*

(*b*) *Connection of 1 kΩ load resistance. Assume* $\eta = 2$. **[GGSIPU, Dec. 2013 (2.5 marks)]**

Solution. Voltage at node $V_1 = 2.1$ V

So corresponding voltage across each diode will be 0.7 V.

Now we know that current across the diode

$$I = I_0 e^{\frac{V}{\eta V_T}} \qquad ...(i)$$

(*a*) When $V = 0.7$ V, then

$$I_1 = \frac{10 - V_1}{1\text{k}\Omega} = \frac{10 - 2.1}{1} = 7.9 \text{ mA}$$

Now from Eq. (*i*), we have

$$I_0 = \frac{I}{e^{\frac{V}{\eta V_T}}} = \frac{7.9}{e^{\frac{0.7}{2V_T}}} = 7.9\, e^{-\frac{0.7}{2V_T}} \qquad ...(ii)$$

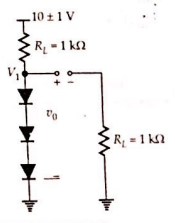


Figure 3.43

Now when $V_{CC} = 10 + 1 = 11$ V, then current through each diode

$$I_2 = \frac{11 - 2.1}{1\text{k}\Omega} = 8.9 \text{ mA}$$

So $$8.9 = I_0 = e^{\frac{V'}{\eta V_T}} \qquad ...(iii)$$

Putting the value of I_0 from Eq. (*ii*) in Eq. (*iii*)

$$8.9 = 7.9\, e^{-\frac{0.7}{2V_T}} e^{\frac{V'}{\eta V_T}} = 7.9\, e^{\frac{V' - 0.7}{2V_T}}$$

Taking log $\log_e 8.9 = \log 7.9 + \dfrac{V'-0.7}{2V_T}$

or $\dfrac{V'-0.7}{2V_T} = \log_e \dfrac{8.9}{7.9}$

or $V' = 2V_T \log \dfrac{8.9}{7.9} + 0.7$

For one-diode $V' = 0.7 + 2V_T \log_e (1.12)$

For three-diode $V_1' = 2.1 + 6V_T \log_e (1.12)$

Total voltage $V' = 3V'$

Percentage change

$$= \frac{V_1' - V}{V} \times 100$$

$$= \frac{6V_T \log(1.12) - 2.1}{2.1} = \frac{6 \times 26 \times 10^{-1}}{2.1} \log(1.12) = \mathbf{0.84\%}$$

(*b*) When 1 kΩ is connected across load (V_S = +10 V)

Then current through load $I_L = \dfrac{2.1\text{ V}}{1\text{k}\Omega} = 2.1\text{ mA}$

Then current flowing through diodes $I' = 7.9 - 2.1 = 5.8$ mA

$\therefore$ $I' = I_0 e^{V'/2V_T}$

Therefore total percentage change in the regulated voltage can be obtained as in case (*a*), which gives % change in voltage

$$= \frac{\Delta V}{V} \times 100 = \frac{V_1' - V_1}{V_1} \times 100$$

$$= \frac{6V_T}{2.1} \ln \frac{7.9}{5.8} \times 100 = \frac{6 \times 26 \times 10^{-1}}{2.1} \ln 1.36 = \mathbf{2.28\%}$$

Problem 3.10 *The current voltage characteristics of PN-junction is given by the relation :*

$$I = I_0 \left[\exp \frac{eV}{\eta k_B T} - 1 \right]$$

The diode current is 0.5 mA at V = 340 mV and 15 mA at V = 440 mV. Determine the value of η. *Assume* $\dfrac{k_B T}{e} = 25\,mV$.

Solution. Given :

$I_1 = 0.5\text{ mA} = 0.5 \times 10^{-3}\text{ A}$; $V_1 = 340\text{ mV}$, $I_2 = 15\text{ mA} = 15 \times 10^{-3}\text{ A}$,

$V_2 = 440\text{ mV}$ and $\dfrac{k_B T}{e} = 25\text{ mV}$

We know that the diode current I_1

$$0.5 \times 10^{-3} = I_0 \left[\exp \frac{eV_1}{\eta k_B T} - 1 \right]$$

$$= I_0 e^{eV_1/\eta k_B T} = I_0 e^{340/25\eta} = I_0 . e^{13.6/\eta} \quad \ldots(i)$$

Similarly, the diode current (I_2)

$$15 \times 10^{-3} = I_0 e^{440/25\eta} = I_0 e^{17.6/\eta} \quad \ldots(ii)$$

Dividing Eq. (*ii*) by Eq. (*i*)

$$30 = e^{(17.6-13.6)/\eta} = e^{4/\eta}$$

Taking natural logarithms on both sides

$$\log_e 30 = \log_e (e^{4/\eta}) = \frac{4}{\eta} \log_e e = \frac{4}{\eta}$$

or $3.4 = \dfrac{4}{\eta}$ or $\eta = \dfrac{4}{3.4} = 1.18.$

Problem 3.11 *When the junction temperature of a Ge diode increases from 30° C to 85° C, by what factor will the reverse saturation current increase ?*

Solution. Experimentally it has been observed that the increase of reverse saturation current for bath Ge and Si diodes is 7% per degree centigrade rise in temperature. This leads to the fact that the reverse saturation current increases by a factor of two for 10° C rise in temperature. Thus if $I_0(t)$ and $I_0(t)$ are reverse saturation currents at t° C and t_0° C respectively then these currents should be related by the following analytical expression :

$$I_0(t) = I_0(t_0) \times 2^{(t-t_0)/10}$$

$\therefore$ $I_0(85°) = I_0(30°) \times 2^{(85-30)/10} = I_0(30°) \times 2^{5.5} = 45.25 I_0(30°)$

$\therefore$ $\dfrac{I_0(85°)}{I_0(30°)} = 45.25$

Problem 3.12 *A germanium diode has a saturation current of 10 μA at room temperature (i.e., 300 K). Find the saturation current at 400 K.*

Solution. Given : $I_{300} = 10\,\mu\text{A} = 10 \times 10^{-6}\text{ A} = 1.0 \times 10^{-5}\text{ A}$, $T_1 = 300$ K and $T_2 = 400$ K

We know that saturation current at 400 K

$$I_{400} = I_{300} \times 2^{(T_2 - T_1)/10}$$

$$= 10 \times 10^{-6} \times 2^{(400-300)/10}$$

$$= 10 \times 10^{-6} \times 2^{10} = 10.2\text{ mA}.$$

Conceptual Questions

3.1 *What are the various forces acting on charge carriers in a P-N junction ?*

Ans. There are two types of forces – one due to diffusion of carriers and another due to electric field created in the space region of the *P-N* junction.

3.2 *What is an ideal PN-junction diode ?*

Ans. An ideal diode has zero resistance when forward biased and infinite resistance when reverse biased. It acts like an open switch in reverse bias and closed switch in forward bias.

3.3 *Define knee voltage or cut-in-voltage from current voltage characteristics of a PN-junction diode.*

Ans. The forward bias characteristics of a *PN-junction diode indicate that practically no diode current flows till the point A in the characteristics is reached. As the forward voltage increases beyond the point A the current increases rapidly. The voltage at which the diode starts conducting is known as knee voltage* or cut-in voltage, which can be obtained from the forward characteristics by extending the part *BA* of the curve backwards until it meets the voltage axis. The value of the voltage where the curve meets the voltage axis is equal to knee voltage (V_K) as shown in Fig. 3.44. Its value is 0.6 V for silicon diodes and 0.2 V for germanium diodes.

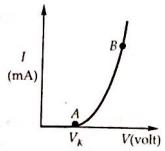


Figure 3.44

3.4 *Distinguish between Zener breakdown and Avalanche breakdown.*

Ans.

S.No.	Zener breakdown	Avalanche breakdown
1.	This type of breakdown occurs in heavily doped *P-N* junction.	This breakdown occurs in lightly doped junction.
2.	The phenomenon is caused by tunneling or field emission.	The phenomenon is caused by impact ionization and avalanche multiplication.
3.	Breakdown voltage is low.	Breakdown voltage is high.
4.	Temperature coefficient of breakdown voltage is negative.	Temperature coefficient of breakdown voltage is positive.

3.5 *Discuss biasing of a PN-junction diode using Fermi level diagram.*

Ans. Biasing of PN-Junction

(*a*) **PN-Junction in Equilibrium (No bias).** When *PN*-junction is in equilibrium, the number of carriers diffusing from *P*-side to *N*-side is equal to the number of carriers diffusing from *N*-side to *P*-side. Consequently, there is no current across the junction. [Fig. 3.45(*a*)]

(*b*) **PN-Junction with Forward Bias.** In Fig. 3.45(*b*), forward bias connections are shown, *P*-side is connected to the positive of the battery. Due to the external bias, equilibrium conditions are disturbed and, therefore, energy bands and the Fermi level altered. Since, in this case, negative of the

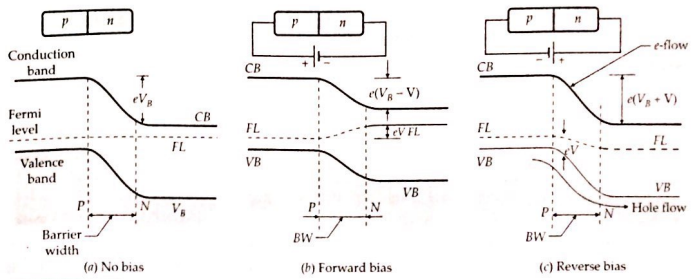


Figure 3.45 Biasing of *P-N* junction.

battery is connected to *N*-type side, energy of the electrons in *N*-type region increased by an amount eV, here *V* is voltage applied by the battery. Consequently, as shown in Fig. 3.45(*b*), Fermi level rises by eV and their energy bands adjust their position so as to suit the elevation of Fermi level. Due to increase in energy on *N*-side potential barrier is reduced to $e(V_B - V)$. The net result is that the electrons crossing the junction from *N*-side will not face a low potential barrier and a small width of space charge region. Consequently, they can easily cross the junction. Since electrons in *N*-side are in majority, current across the junction increases.

(*c*) **PN-junction with Reverse Bias.** Connections are shown in Fig. 3.45(*c*), *N*-side is connected to the positive battery. It lowers the Fermi level on *N*-side by an amount eV raising the barrier height $e(V_B + V)$ and increasing the depletion width too. The electrons that are in majority in *N*-side will now face larger width of space charge region. Therefore, number of electrons crossing the junction from *N*-side to *P*-side decreases. Consequently, current is very much reduced in reverse biasing of the *PN*-junction.

3.6 *What is depletion layer ?*

Ans. When a *PN*-junction is formed, there is a difference of concentration of charge carriers in two regions. This causes diffusion of charge carriers. Holes diffuse from *P* to *N* region and electrons from *N* to *P* region. As *N*-region is very rich in free electrons, therefore the holes diffused into *N*-region recombine with electrons in the vicinity of the junction. Similarly, *P*-region is very rich in holes and therefore the electrons diffused into *P*-region recombine with holes in the vicinity of the junction. Consequently, there are no mobile charge carriers such as free electrons and holes in a narrow region of width $\approx 10^{-6}$ m at the junction. That is why this region is called depletion layer or transition layer.

3.7 *What is potential barrier ?*

Ans. For a *PN*-junction, a barrier is set up against further movement of charge carriers *i.e.*, holes and free electrons. This is known as potential barrier or junction barrier.

3.8 *Write diode current equation.*

Ans. The current flowing through a *PN*-junction diode due to application of a voltage *V* across the junction is given by

$$I = I_0\left[\exp\frac{Ve}{\eta k_B T} - 1\right]$$

where I_0 = reverse saturation current in Ampere at temperature T K,

e = electronic charge = 1.6×10^{-19} C,

k_B = Boltzmann constant,

T = Temperature in K,

and η = Constant (1 for Ge and 2 for Si)

3.9 *Define ac and dc resistance. Draw the necessary graph in this context.*

[GGSIPU, Oct. 2013 (2-5 marks)]

Ans. *Two* types of diode resistances are often defined depending upon the mode of operation :

(*i*) *Static resistance or dc resistance* (r_{dc}). If only a steady dc current flows through the diode, its resistance is called static resistance.

Mathematically,

$$r_{dc} = \frac{\text{Applied voltage } (V)}{\text{Steady current } (I)}$$

(*ii*) *Dynamic resistance or ac resistance* (r_{ac}). The dynamic resistance r_{ac} is defined as the ratio of a small change in applied voltage to the corresponding change in diode current *i.e.*,

$$r_{ac} = \frac{\Delta V}{\Delta I}.$$

For graph refer to Figs. 3.15 and 3.16 at page 97-98.

3.10 *Discuss capacitive effects in PN-junction diode.*

Ans. There are *two* types of capacitive effects in *PN*-junction diode :

(*i*) *Space Charge or Transition Capacitance* (C_T). As we know that the thickness of depletion layer changes with voltage applied across the junction. Reverse biasing of a *PN*-junction causes majority carriers to move away from the junction, therefore uncovering more immobile charges. This increases the thickness of depletion layer. Similarly, the forward biasing of a *PN*-junction decreases the amount of uncovered charge and hence the thickness of depletion layer. This change is uncovered charge with applied voltage may be considered as a capacitive effect. It gives rise to transition capacitance C_T.

$$C_T = \frac{dQ}{dV} = \frac{\varepsilon A}{x}$$

The transition capacitance is not constant but depends on applied voltage and hence it is also known as *voltage variance capacitance.*

(*ii*) *Diffusion or Storage Capacitance* (C_D). When forward biased the PN junction ...

3.11 *What is rectifier ? Write types of rectifiers.*

Ans. Rectifier is a circuit employing one or more diodes to convert a.c. voltage into pulsating d.c. voltage. There are *three* types of rectifiers :

(*i*) Half wave rectifier (*ii*) Full wave rectifier (*iii*) Bridge type rectifier

3.12 *What do you mean by Clippers and Clampers ?*

Ans. *Clipper.* Clipper circuits remove part of the waveform and are of four types : positive, negative, biased and combination.

Clamper. The circuit with which the waveform can be shifted such a way that a particular part of it (say positive or negative peak) in maintained at a specified voltage level, is known as clamper.

Exercises

Theoretical Questions

3.1 Differentiate between clippers and clampers using suitable circuit diagrams. **[GGSIPU, Dec. 2013 (2.5 marks)]**

3.2 What is meant by the breakdown region of diode ? **[GGSIPU, Dec. 2013 (2.5 marks)]**

3.3 Define peak inverse voltage. What are the values of PIV for half wave and full wave rectifier using ideal diode and sinusoidal input ? **[GGSIPU, Dec. 2013 (6.5 marks)]**

3.4 Compare the performance of half wave rectifier and full wave rectifier using suitable circuit diagrams and expressions. **[GGSIPU, Dec. 2013 (6.5 marks)]**

3.5 Discuss full wave rectifier. Derive expressions for ripple factor and rectification efficiency of half and full wave rectifier. **[GGSIPU, Dec. 2013 (6.5 marks)]**

3.6 Differentiate transition and diffusion capacitance. **[GGSIPU, Dec. 2013 (2.5 marks)]**

3.7 Explain the term ripple factor and PIV for diode. **[GGSIPU, Nov. 2013 (2 marks)]**

3.8 Draw the circuit diagram of a bridge full wave rectifier. Explain its working and also find its efficiency. **[GGSIPU, Nov. 2013 (5 marks)]**

3.9 Explain the operation of positive and negative clamper using *PN*-junction diode with the help of diagram. **[GGSIPU, Nov. 2013 (2.5 marks)]**

3.10 Explain the effect of temperature of *VI*-characteristic of *PN*-junction diode. **[GGSIPU, Oct. 2013 (2.5 marks)]**

3.11 Explain the working of *PN*-junction diode with the help of suitable diagram. **[GGSIPU, Oct. 2013 (2.5 marks)]**