BIPOLAR JUNCTION TRANSISTORS

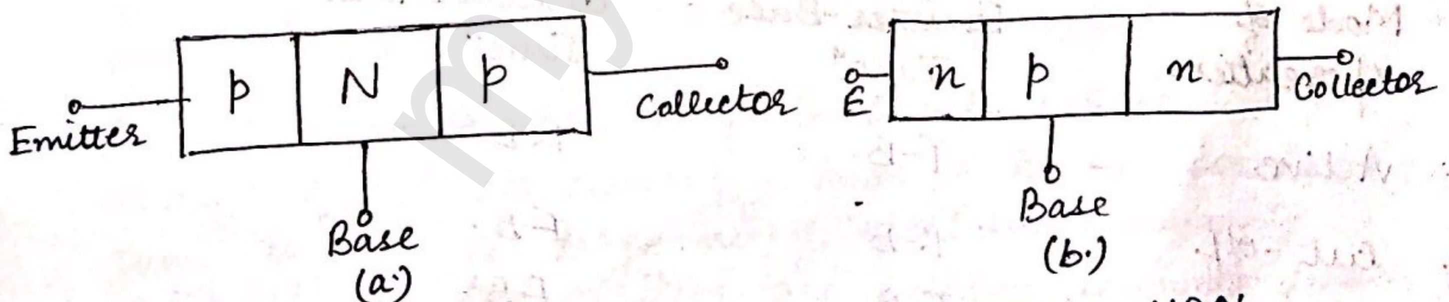
A semiconductor device consisting of two p-n junc^n formed by sandwitching either p-type or n-type semiconductor b/w a pair of opposite types is known as a transistor.

It is also known as Bipolar Junc^n transistor (BJT) since its operation depends upon the interaction of both the majority and minority carriers.

Merits :-
(i) higher efficiency
(ii) more mechanical strength
(iii) light in weight
(iv) smaller in size
(v) smaller power consumption etc

CONSTRUCTION OF TRANSISTOR

It consists of two PN-junc^n diodes, which are cemented back to back or front-to-front. In other words, it may either have a N-type semiconductor sandwitched b/w two P-type semiconductors or a P-type semiconductor inserted b/w two N-type semiconductors.



Two arrangements are referred as PNP or NPN transistors (as shown in fig. ⓐ and ⓑ)

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The BJT (PNP or NPN transistor) has three regions - emitter, base and collector and having two junc^n's i.e. emitter- base and collector- base.

1. EMITTER :- This region is the heavily doped region as compared to base and collector. The size of emitter is more than base but less than the collector.

2. BASE: The size of base region is extremely small, it is less than emitter as well as the collector. The doping intensity of base is also less than emitter and collector.

3. COLLECTOR: The collector terminal is moderately doped, and the size of collector region is slightly more than emitter region.

BJT BIASING

Different modes of transistor operation depends upon the bias cond^n of each of the two junc^n's namely, emitter- base and collector-base junc^n.

	Mode of Operation	Emitter-Base Junc^n	Collector-Base Junc^n
1.	Active	F.B.	R.B.
2.	Cut - off	R.B	F.B.
3.	Saturation	F.B.	F.B.

* In Amplifiers and oscillators circuits, transistors must operate in active mode, whereas in Switching and other logical circuits, transistors must operate in either cut-off or in saturation mode.

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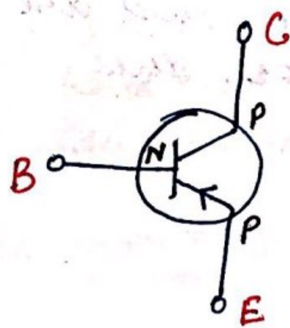
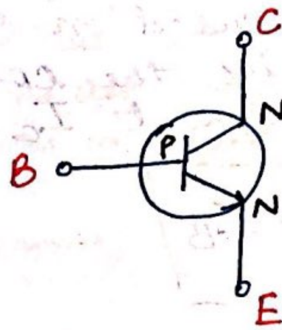
Circuit Symbols of PNP and NPN bipolar transistors :-



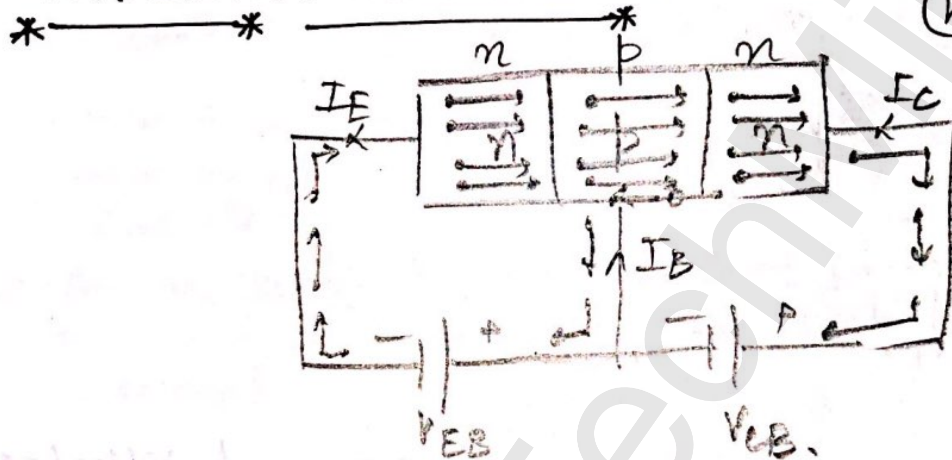
(a.) PNP



(b.) NPN

TRANSISTOR OPERATION

(Working of n-p-n transistor)



1. An n-p-n transistor circuit is shown in above fig. Emitter-Base junc^n is F.B. while collector-base junc^n is R.B.

- The F.B. voltage V_{EB} is quite small whereas R.B. voltage V_{CB} is considerably high. As Emitter-base junc^n is F.B. a large no. of electrons (majority carriers) in the emitter are pushed towards base. This consitutes the emitter current I_E

- When these electrons enters the p-type material (Base) they tend to combine with holes, since the base is lightly doped and very thin, only a few electrons (less than 5%.) combines with holes to constitute the base current I_B

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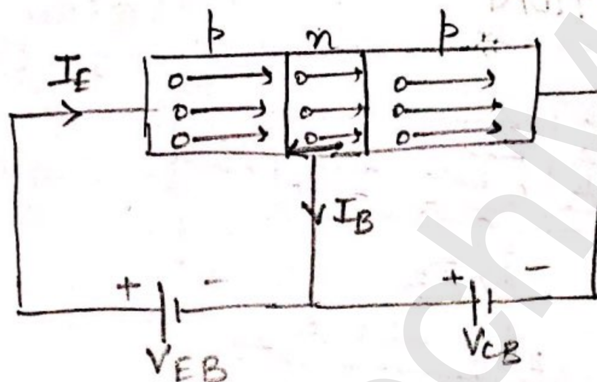
The remaining electrons (more than 95%) diffuse across the thin base region and reach the collector space charge layer. These electrons combines under the influence of +vely biased n-region and are attracted or collected by the collector. This consitutes collector current I_C

$$\therefore \boxed{I_E = I_C + I_B}$$

WORKING OF PNP TRANSISTOR



In this the emitter-base junc^n is F.B and collector-base junc^n is R.B. V_{EB} is quite small whereas V_{CB} is considerably high. As the emitter-base junc^n is F.B. a large no. of holes in the emitter are pushed towards the base, which constitutes to I_E. When these holes enters p-type material (base) they tend to combine with electrons. Since the base is lightly doped and very thin only a few electrons (less than 5%) combine with electrons to constitute base current I_B.

The remaining holes (more than 95%) diffuse across the thin base region and reach the collector space charge layer, which constitutes to I_C

$$\boxed{I_E = I_B + I_C}$$

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* Most of the transistors are n-p-n type and not p-n-p type because in n-p-n transistors the current conduction is mainly due to electrons whereas in p-n-p transistors the current conduction is mainly by holes. As electrons are more mobile than holes we can have conduction in n-p-n transistors.

TRANSISTOR CONFIGURATION

The BJT can be connected in 3 ways in a circuit as follows:-

(i) Common emitter (CE) configuration in which emitter terminal is common b/w input (base) and output (collector) circuits.

(ii) Common Base (CB) configuration in which base terminal is common b/w input (emitter) and output (collector) circuits

(iii) Common Collector (CC) configuration, in which collector terminal is common b/w input (base) and o/p (emitter) circuits.

COMMON BASE CONFIGURATION

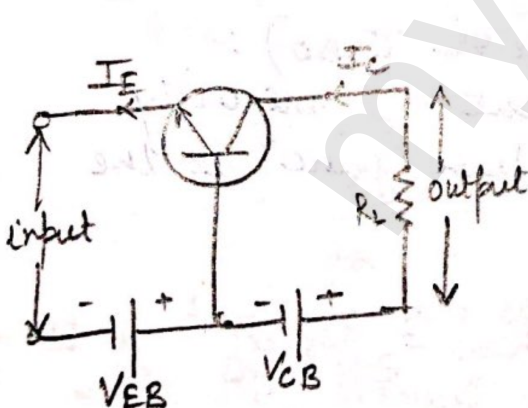

fig.(1)

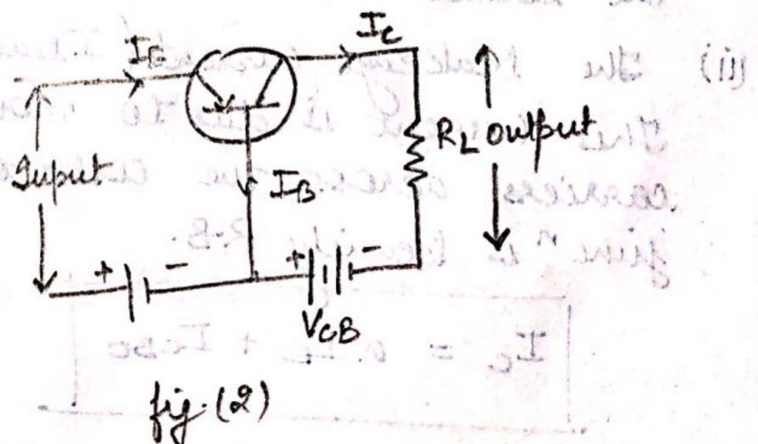

fig.(2)

The common base circuit arrangement for n-p-n transistor and p-n-p transistor is shown in fig.(1) and (2)

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Current Amplification factor (α) :- (Ratio of o/p current to i/p current)

α is defined as the ratio of change in collector current to change in emitter current at constant V_{CB}.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \Bigg|_{V_{CB} = \text{constant}}$$

We know that,

$$I_E = I_C + I_B$$

$$\therefore \Delta I_E = \Delta I_C + \Delta I_B$$

$$\frac{\Delta I_E}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_E} + \frac{\Delta I_B}{\Delta I_E}$$

$$1 = \alpha + \frac{\Delta I_B}{\Delta I_E}$$

$$\therefore \alpha = 1 - \frac{\Delta I_B}{\Delta I_E}$$

Practical values of α in commercial transistors is 0.95 to 0.99.

Collector Current :-

Total collector current consists of :-

(i) A large percentage of emitter current that reaches the collector terminal i.e. αI_E

(ii) The leakeage current ($I_{leakeage}$ or I_{CBO}) :-
This current is due to movement of minority carriers across the collector base junc^n as the junc^n is heavily R.B.

$$I_C = \alpha I_E + I_{CBO}$$

I_{CBO} = Collector to base reverse saturation current.

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COMMON COLLECTOR CONFIGURATION

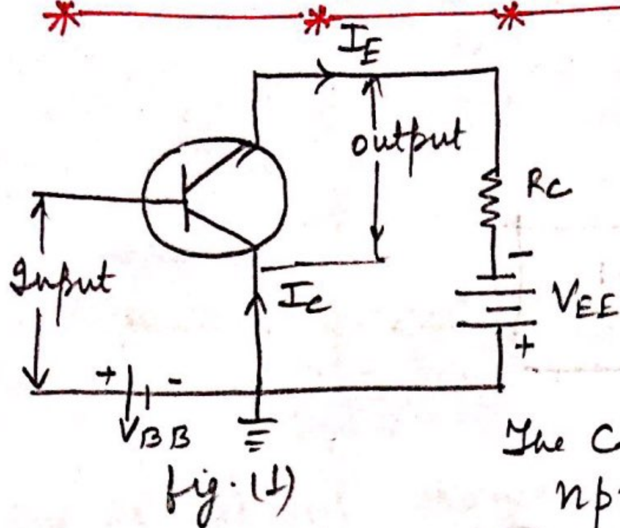

fig. (1)

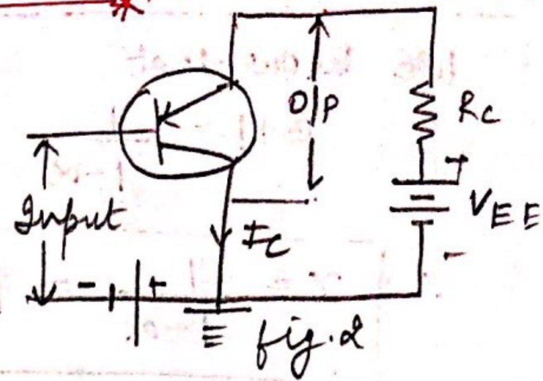

fig. 2

The CC circuit arrangement for npn & pnp transistor is shown in fig 1 and fig 2

Current Amplification factor :-

$$\gamma = \frac{\text{o/p current}}{\text{i/p current}}$$

$$\boxed{\gamma = \frac{I_E}{I_B}}$$

Relation b/w γ and α :-

$$\gamma = \frac{I_E}{I_B} \quad \text{and} \quad \alpha = \frac{I_C}{I_E}$$

Also $I_E = I_C + I_B$

$$I_B = I_E - I_C$$

$$\gamma = \frac{I_E}{I_E - I_C}$$

dividing numerator & denominator by I_E on R.H.S

$$\gamma = \frac{I_E/I_E}{I_E/I_E - I_C/I_E} = \frac{1}{1-\alpha}$$

$$\therefore \boxed{\gamma = \frac{1}{1-\alpha}}$$

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Relation b/w α, β and γ :-

We know that

$$\beta + 1 = \frac{1}{1-\alpha}$$

$$\therefore \boxed{\gamma = \frac{1}{1-\alpha} = \beta + 1}$$

Collector current :-

$$I_C = \alpha I_E + I_{CBO} \quad \text{--- (1)}$$

$$I_E = I_C + I_B \quad \text{--- (2)}$$

putting (2) in (1)

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{I_C = \beta I_B + \gamma I_{CBO}}$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CBO}}$$

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COMMON EMITTER CONFIGURATION

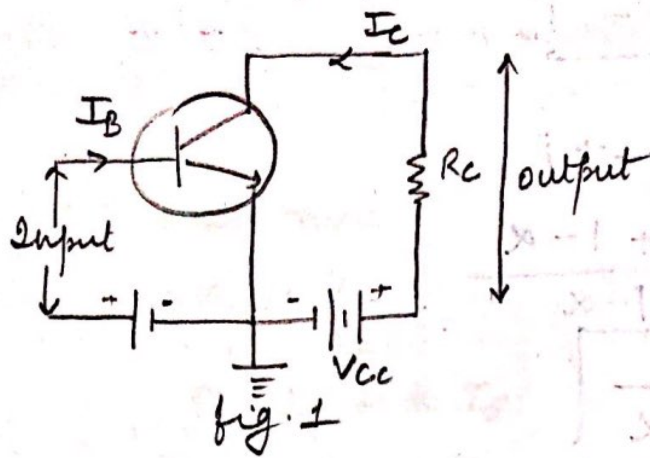

fig. 1

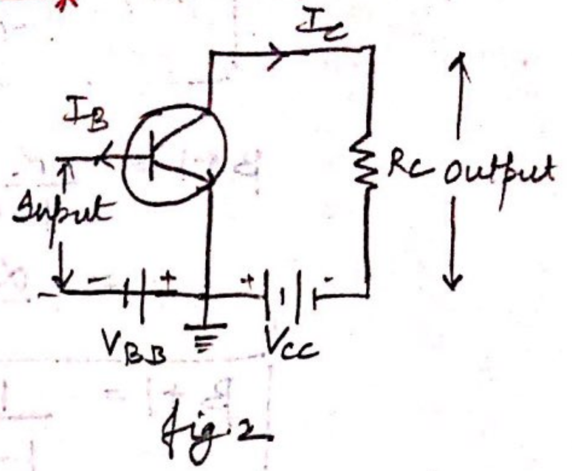

fig. 2

The CE circuit arrangement for n-p-n transistor and p-n-p transistor is shown in fig. 1 and fig. 2

Current Amplification factor (β):-

$$\beta = \frac{\text{o/p current}}{\text{i/p current}}$$

$$\beta_{dc} = \frac{I_C}{I_B} \quad \text{and} \quad \beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

$$\boxed{\beta = \frac{I_C}{I_B}}$$

Relation b/w α and β

we know that

$$\beta = \frac{I_C}{I_B} \quad \text{and} \quad \alpha = \frac{I_C}{I_E}$$

$$\Rightarrow I_E = I_C + I_B$$

$$I_B = I_E - I_C$$

$$\beta = \frac{I_C}{I_E - I_C} \times \frac{I_E}{I_E}$$

$$= \frac{I_C / I_E}{1 - I_C / I_E}$$

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$$\therefore \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1$$

$$= \frac{\alpha + 1 - \alpha}{1-\alpha}$$

$$\boxed{\beta + 1 = \frac{1}{1-\alpha}}$$

Collector current :-

$I_E = I_C + I_B$ and $I_C = \alpha I_E + I_{CBO}$

$$\therefore I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{I_C = \beta I_B + (\beta + 1) I_{CBO}}$$

If $I_B = 0$, I_C is abbreviated as I_{CEO}

I_{CEO} = collector emitter current with base open

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{\therefore I_C = \beta I_B + I_{CEO}}$$

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Ques1 In a CB configuration, the current amplification factor is 0.97. If the emitter current is 1mA, determine the value of base current

Soln We know that

$$\alpha = \frac{I_C}{I_E}$$

or $I_C = \alpha I_E$

$\alpha = 0.97$, $I_E = 1mA$

$I_C = 0.97mA$

$I_E = I_C + I_B$

$I_B = I_E - I_C = 1 - 0.97$

$\therefore I_B = 0.03\ mA$

Ques2 The emitter current I_E in a transistor is 3mA. If the leakage current I_{EBO} is 5μA and $\alpha = 0.98$. Calculate I_C and I_B (for CB configuration)

$I_C = \alpha I_E + I_{CBO}$

$\alpha = 0.98$

$I_E = 3mA$ and $I_{CBO} = 5\mu A = 0.005mA$

$\therefore I_C = 0.98 \times 3 + 0.005$

$I_C = 2.945mA$

$I_E = I_C + I_B$

$I_B = I_E - I_C$

$I_B = (3 - 2.945)\ mA$

$I_B = 55\mu A$

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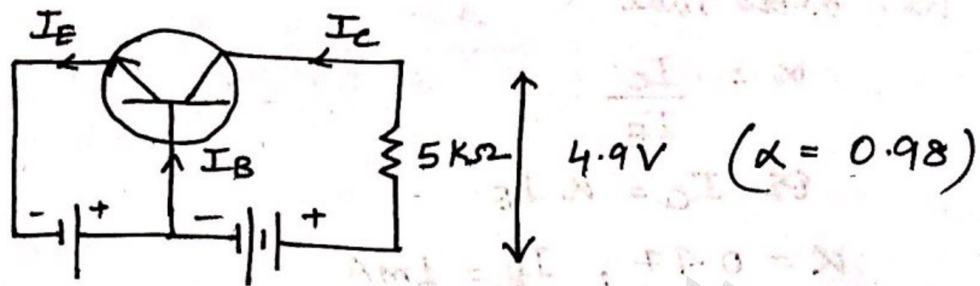
Ques 3. In CB configuration the value of $\alpha = 0.98$. A Voltage drop of 4.9V is obtained across a resistor 5kΩ when connected in collector circuit. Find I_B.



$$I_C = \frac{4.9}{5k\Omega} = 0.98mA \quad ; \quad \alpha = \frac{I_C}{I_E}$$

$$I_E = \frac{I_c}{\alpha} = \frac{0.98\ mA}{0.98} = 1mA$$

$$I_E = I_B + I_c$$

$$I_B = I_E - I_c$$

$$= 1 - 0.98$$

$$\boxed{I_B = 0.02mA}$$

Ques 4. calculate the Value of emitter current in a transistor for which $\beta = 40$ and $I_B = 25\mu A$ (for CE configuration)

$\beta = 40$

$I_B = 25\mu A$

$I_E = ?$

$$\beta = \frac{I_c}{I_B}$$

$$I_C = \beta I_B = 40 \times 25 = 1000\mu A$$

$$I_E = I_c + I_B$$

$$= 1000 + 25$$

$$I_E = 1025\mu A = 1.025mA \text{ Ans}$$

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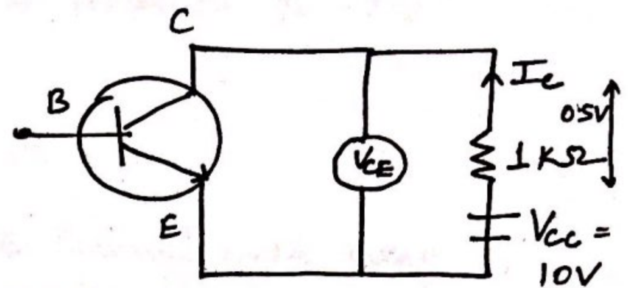
Ques5. In a CE configuration the collector supply Voltage is 10V. when a resistor $R_C = 1 k\Omega$ is connected in a collector circuit, the Voltage drop across it is 0.5V, For $\alpha = 0.98$, determine

(i) V_{CE}

(ii) I_B.



$$V_{CE} = V_{CC} - \text{drop in } R_C$$

$$= 10 - 0.5 = 9.5V$$

$$\therefore \boxed{V_{CE} = 9.5V}$$

$I_B = ?$

$$\beta = \frac{I_c}{I_B}$$

$$I_B = \frac{I_c}{\beta}.$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_c = \frac{0.5}{1k\Omega} = 0.5\,mA$$

$$I_B = \frac{0.5\,mA}{49}$$

$$\boxed{I_B = 0.0102\,mA} \text{ Ans.}$$

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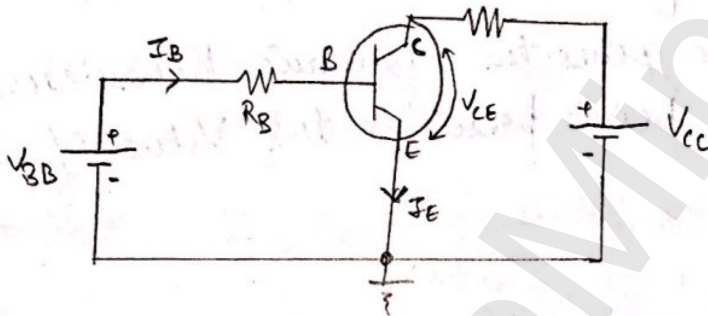
TRANSISTOR LOAD LINES

It is defined as the locus of operating point on the output char. of the transistor. It is the line on which operating point moves when ac signal is applied to the transistor

dc load line

Let us consider a CE amplifier circuit with base resistor R_B and collector resistor R_C



In the output ckt, apply KVL:

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \quad \text{——— (1)}$$

As, V_{CC} & R_C are constant fixed values i.e. $\frac{V_{CC}}{R_C}$ is constant

∴ eqn (1) represents a straight line eqn $y = mx + c$

where m = slope of line $= \frac{-1}{R_C}$ &

$\frac{V_{CC}}{R_C}$ = intercept of line on the vertical current axis of o/p char.

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consider, (i) when $I_C = 0$

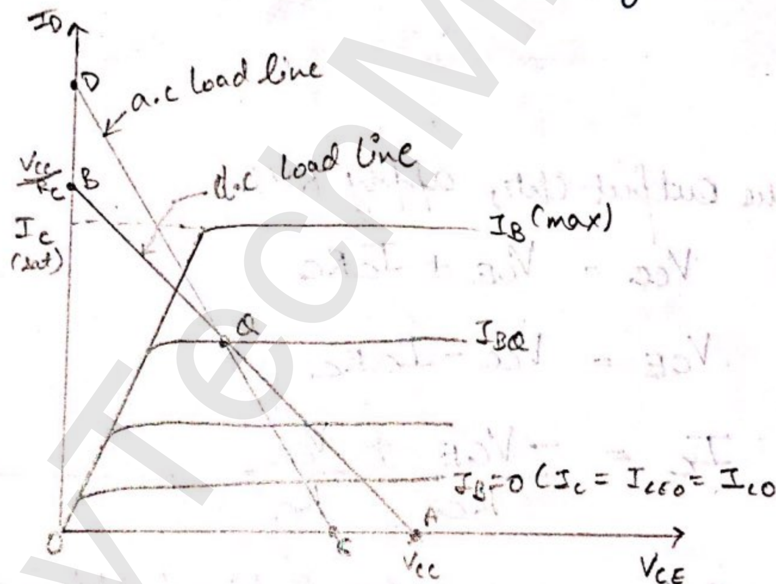
$V_{CE} = V_{CC}$; Cut-off pt A

(ii) when $V_{CE} = 0$

$I_C = \frac{V_{CC}}{R_C}$; Saturation pt. B

The dc load line is given by joining pts A and B. The intersection of dc load line and characteristic curve gives the operating point (or Q-point or quiescent point)

* The dc load line gives the dynamic behaviour of the Circuit and Q-point provides the Value of I_C and V_{CE}.



ac load line

On applying the ac signal to the input, Q-point remains stable while transistor voltage V_{CE} and collector current I_C vary about the point.

If we draw ac load line, it has steeper slope than the dc load line but two lines will intersect at the Q-point.

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The effective ac load Resistance, R_{ac} =

$$\frac{1}{R_{ac}} = \frac{1}{R_C} + \frac{1}{R_L} \quad (R_L || R_C)$$

$$= \frac{R_L + R_C}{R_C R_L}$$

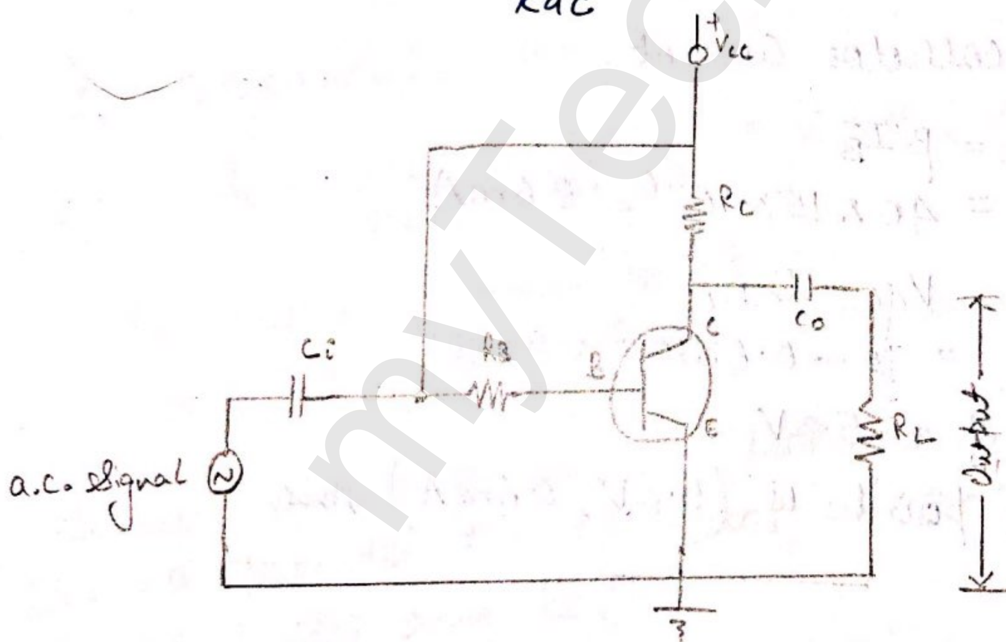
$$\therefore R_{ac} = \frac{R_C R_L}{R_C + R_L} \quad (\because R_C < R_L)$$

$$\Rightarrow R_{ac} = R_C$$

To draw ac load line, max. V_{CE} and max. I_C is required in presence of ac signal

$$V_{CE} = V_{CEQ} + I_{CQ} R_{ac} \quad \text{(cut-off point C)}$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \quad \text{(Saturation point D)}$$



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Ques. In CE configuration, $V_{CC} = 10V$, R_L is $8k\Omega$. Draw dc load line. Determine the Q-pt for zero signal if base current is $15\mu A$ and $\beta = 40$

$V_{CC} = 10V$

$R_L = 8k\Omega$

I_B (zero signal base current) $= 15\mu A$

$\beta = 40$

for CE configuration

$$V_{CE} = V_{CC} - I_C R_C$$

for $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_L} = 1.25mA \text{ (pt A on load line)}$$

for $I_C = 0$, $V_{CE} = V_{CC} = 10V$ (pt B on load line)

Zero signal collector current

$$I_C = \beta I_B$$
$$= 40 \times 15 \times 10^{-6} = 0.6mA$$

$$V_{CE} = V_{CC} - I_C R_L$$
$$= 10 - 0.6 \times 10^{-3} \times 8 \times 10^{3}$$
$$= 5.2V$$

$\therefore$ Operating point is $(5.2V, 0.6mA)$ Ans.

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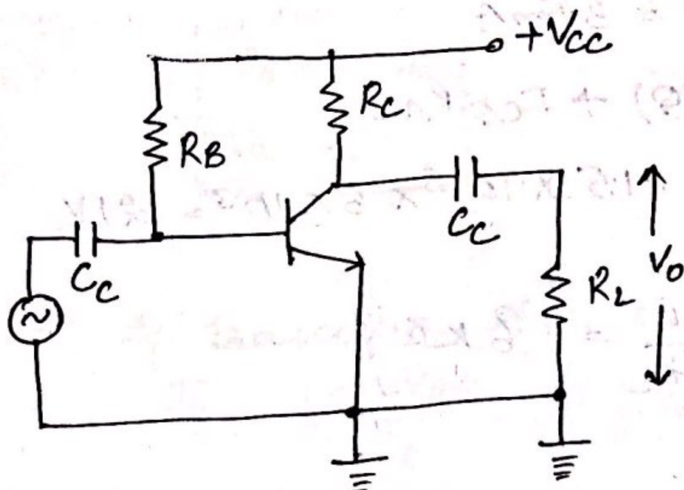
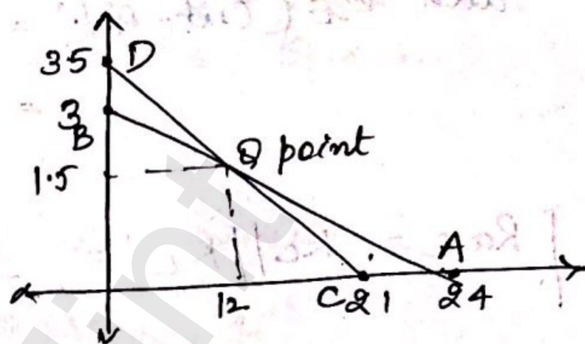
Ques 2. In a transistor amplifier as shown in fig., $R_C = 8 K\Omega$, $R_L = 24 K\Omega$ and $V_{CC} = 24V$.
Draw the dc load line, determine the optimum operating point. Also draw the ac load line.





Solⁿ:- Given $R_C = 8 K\Omega$
$R_L = 24 K\Omega$
$V_{CC} = 24V$

(a.) I_C (saturation), when $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3mA$$ (point B on dc load line)

V_{CE} (Cut-off) when $I_C = 0$
$V_{CE} = V_{CC} = 24V$ (point A on dc load line)

(b.) Optimum operating point :- Midway of the load line AB provides the optimum or max. operating point $I_C(Q)$ and $V_{CE}(Q)$

$$I_C(Q) = \frac{I_C}{2} = 1.5mA$$

$$V_{CE}(Q) = \frac{24}{2} = 12V$$

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(c) In AC-Load line

$$I_C(\text{saturation}) = I_C(Q) + \frac{V_{CE}(Q)}{R_{ac}}$$

$$= 1.5 + \frac{12}{6 \times 10^3}$$

$$= 3.5\,mA$$

and $V_{CE}(\text{cut-off}) = V_{CE}(Q) + I_{CQ} R_{ac}$

$$= 12 + 1.5 \times 10^{-3} \times 6 \times 10^3 = 21V$$

$$\left[R_{ac} = R_C || R_L = \frac{R_C R_L}{R_C + R_L} = 6\,k\Omega \right]$$

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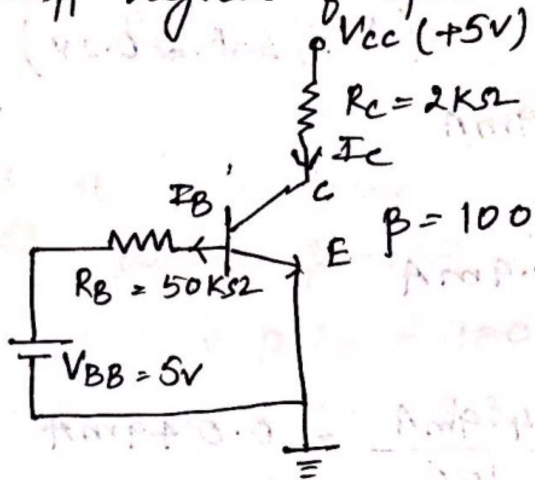
Ques. A circuit is shown in fig. Analyze it for diff. regions of operation.



Given $V_{BB} = 5V$
$V_{CC} = 5V$
$\beta = 100$
$R_C = 2K\Omega$
$R_B = 50k\Omega$

(a.) If transistor operates in active region

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \quad (V_{BE} = 0.7V \text{ for Si})$$

$$I_B = \frac{5-0.7}{50}$$

$$= 0.086mA$$

$$I_C = \beta I_B = 100 \times 0.086 mA = 8.6mA$$

Collector voltage $V_C = V_{CC} - I_C R_C$

$$= 5 - 8.6 \times 2$$

$$= -7.2V$$

Value of V_C is impossible because of +ve V_{CC} and emitter is grounded
so, transistor cannot operate in active region

(b.) Consider the transistor operation in saturation region

$$I_B = \frac{V_{BB} - V_{BE,sat}}{R_B} \quad (V_{BE,sat} = 0.8V)$$

$$= \frac{5-0.8}{50} = 0.084mA$$

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$$I_C = \frac{V_{CC} - V_{CE,sat}}{R_C} \quad (V_{CE,sat} = 0.2V)$$

$$= \frac{10-0.2}{2} = 4.9mA$$

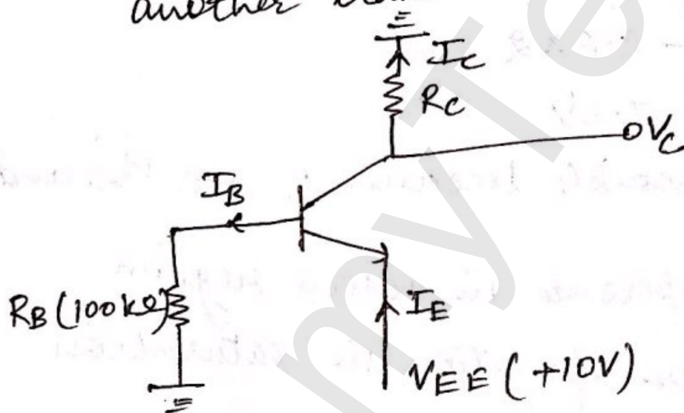
$$= \frac{10-0.2}{2} = 4.9mA$$

$$I_{B,min} = \frac{I_{C,sat}}{\beta} = \frac{4.9mA}{100} = 0.049mA$$

Here $I_B > I_{B,min}$

∴ transistor will definately operate in Saturation region.

Ques. The p-n-p transistor in fig has $\beta = 50$. Find the Value of R_C to Obtain $V_C = +5V$. What happens if the transistor is replaced with another transistor having $\beta = 100$.



(a.) $R_B = 100k\Omega$, $V_{EE} = 10V$, (in active mode) $V_C = +5V$

$V_{BE} = 0.7V$

Apply KVL in input

$$V_{EE} = V_{EB} + I_B R_B$$

$$I_B = \frac{V_{EE} - V_{EB}}{R_B} = \frac{10-0.7}{100} = 0.093mA$$

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$I_C = \beta I_B = 50 \times 0.093 = 4.65 mA$

$\therefore R_C = \frac{V_C}{I_C} = \frac{5}{4.65} = 1.08 K\Omega$

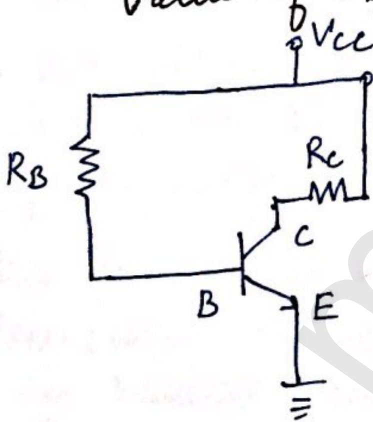
(b.) Ques. If the transistor is replaced by another one having $\beta = 100$

$I_C = \beta I_B = 100 \times 0.093$
$= 9.3 mA$

$V_C = I_C R_C = 9.3 \times 1.08$
$= 10.04 V$

This shows that transistor will operate in saturation region as collector voltage is greater than base voltage

Ques. A fixed bias circuit has $R_C = 3.3 K\Omega$ and $V_{CC} = 15V$. The transistor has a typical current gain of 60 with min. & max. of 30 and 90 resp. Select the value of R_B to give $V_{CE} = 5V$.



Applying KVL

$V_{CC} - I_C R_C - V_{CE} = 0$ —— (1)

$V_{CC} - I_B R_B - V_{BE} = 0$ —— (2)

$30 < \beta < 90$

$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{15 - 5}{R_C}$

$= \frac{10}{3.3 \times 10^3} = 3.03 mA$

Since $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$

Typical value of $\beta = 60$

$\therefore I_B = \frac{3.03 \times 10^{-3}}{60} = 50.5 \times 10^{-6}$ Amp

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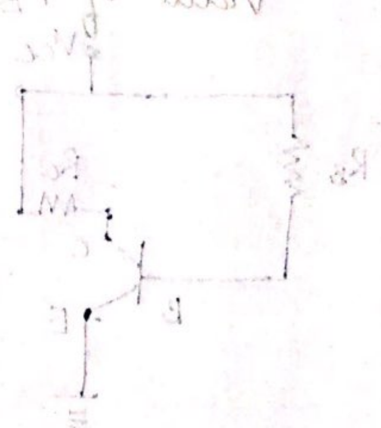
from eqⁿ (2)

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

($V_{BE} = 0.7V$ for Si transistor)

$$= \frac{15 - 0.7}{50.5 \times 10^{-6}} = 283.16 k\Omega$$



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THERMAL RUNAWAY

The collector current (or current gain, β_{dc}) of a transistor strongly depends on two parameters
(i) Transistor
(ii) Temperature

In a circuit, if transistor is replaced by another, then I_C and V_{CE} also change. Similarly I_C (or β_{dc}) Varies with temp. Circuit analysis of transistor indicates that β_{dc} increases with increasing temp and decreases with decreasing temp.

So, for faithful Amplification of input signal, Q-point must remain fixed, irrespective of these variations. This process is known as stabilization.

Thermal Runaway is the process in which collector current increases with temp. As collector current increases, temp. of the junc^n increases due to power dissipation (I^2R) at the collector junc^n. The increases in temp. ΔT increases the collector current therby further increasing in the temp. As a result self-destruction of transistor is possible.

This process is cumalative and fast and may cause the transistor to be destroyed or damaged. Therefore, in any transistor circuit, this effect should be avoided.

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STABILITY FACTOR

In a transistor ckt, it is necessary and desirable to keep I_C and V_{CE} constant so that Q-point becomes stable. There are 2 methods to make operating point fixed.

(i) Stabilization (ii) Compensation

In the first case, biasing ckt is used and in 2nd case temp. sensitive devices such as diodes, thermistors etc. are used to compensate the variations in voltages & currents to keep operating point (I_{CQ}, V_{CEQ}) constant.

Stability factor, S is defined as the rate of change of collector current with respect to I_{CO} current by keeping β_{dc} and V_{CE} constant.

$$S = \left(\frac{\partial I_C}{\partial I_{CO}}\right)_{\beta_{dc} \text{ and } V_{CE}} \approx \frac{\Delta I_C}{\Delta I_{CO}}$$

In CE configuration,

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CO}$$

differentiating with respect to I_C

$$1 = \beta_{dc} \frac{\partial I_B}{\partial I_C} + \frac{(1+\beta_{dc})\,\partial I_{CO}}{\partial I_C}$$

$$S = \frac{1 + \beta_{dc}}{1 - \beta_{dc}\left(\frac{\partial I_B}{\partial I_C}\right)}$$

$$\boxed{S = 1 + \beta_{dc}}$$

for a circuit in which I_B & I_C are independent i.e. $\frac{\partial I_B}{\partial I_C} = 0$

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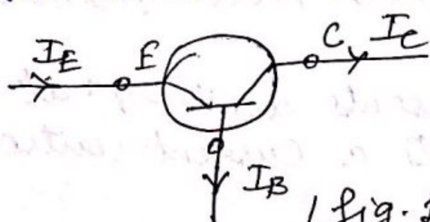
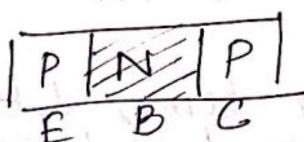
EBER-MOLL'S MODEL

Eber-Moll Model is called the coupled diode model which describes the dc char. of a transistor. This model generalizes the behaviour of a transistor by considering the normal and inverted mode of operations.

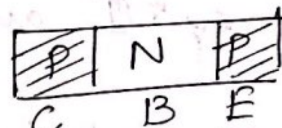
Let us consider the PNP transistors,



(fig. 1)



(Normal operation)



(Inverted operation)

During normal operation, V_{EB} is F.B. and V_{CB} is R.B.

$$I_{EN} = I_{EO}\left(e^{V_{EB}/V_T} - 1\right)$$

and
$$I_{CN} = \alpha_N I_{EN}$$
$$= \alpha_N I_{EO}\left(e^{V_{EB}/V_T} - 1\right)$$

where I_{EO} and α_N are reverse saturation currents at emitter junc^n and current amplification factor in normal operation.

I_{EN} and I_{CN} are emitter & collector current resp. in normal mode.

Under inverted mode, V_{EB} is R.B and V_{CB} is F.B.

$$\therefore\ I_{CI} = -I_{CO}\left(e^{V_{CB}/V_T} - 1\right)$$
$$I_{EI} = \alpha_I I_{CI} = -\alpha_I I_{CO}\left(e^{V_{CB}/V_T} - 1\right)$$

I_{CO} and α_I are reverse saturation currents of diode at collector junc^n and current amplification factor in inverted mode respectively.

I_{EI} and I_{CI} are emitter and collector current resp in the inverted operation.

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$$I_E = I_{EN} + I_{EI}$$
$$= I_{E0}\left(e^{V_{EB}/V_T} - 1\right) - \alpha_I I_{C0}\left(e^{V_{CB}/V_T} - 1\right) \quad (1)$$

and
$$I_C = I_{CN} + I_{CI}$$
$$= -I_{C0}\left(e^{V_{CB}/V_T} - 1\right) + \alpha_N I_{E0}\left(e^{V_{EB}/V_T} - 1\right) \quad (2)$$

eqn (1) and (2) are known as Eber-Moll equations

I_E contains two terms, 1st represents diode eqn at emitter junc^n and 2nd represents a current controlled by collector diode.
Similarly, first terms of I_C represents the diode eqn at collector junc^n and 2nd term is for current controlled by emitter diode.

$$I_{EN} = I_{E0}\left(e^{V_{EB}/V_T} - 1\right)$$

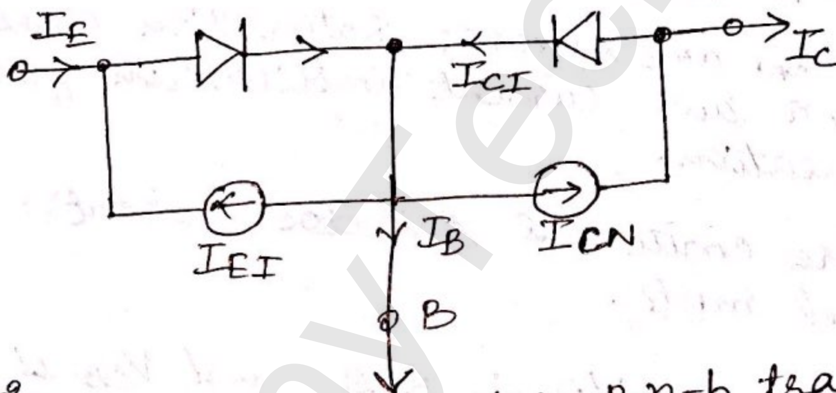

fig 2. Eber-Moll Model of a p-n-p transistor

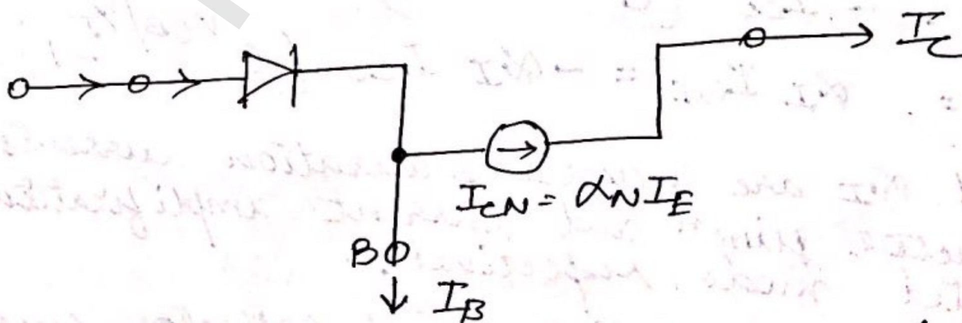

fig. 3. Eber Moll-Model for normal P-N-P Operation

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For a p-n-p transistor in normal mode, C-B arrangement,

V_{EB} = F.B. and V_{CB} = R.B.

Hence $I_{CI} = 0$ (collector-base diode behaves as open)

and $I_{EI} = 0$

Thus Eber-Moll equivalent circuit is shown in fig.3

Also $\alpha_N I_{EO} = \alpha_I I_{CO}$ (Acc. to Reciprocity cond^n of BJT.)

$$\therefore I_E = I_{EO}(e^{V_{EB}/V_T} - 1) - \alpha_I [\alpha_N I_{EO} e^{V_{EB}/V_T} - 1) - I_C]$$

$$= \alpha_I I_C + (1 - \alpha_N \alpha_I) I_{EO} (e^{V_{EB}/V_T} - 1)$$

$$\Rightarrow I_E = \alpha_I I_C + I_{REO} (e^{V_{EB}/V_T} - 1)$$

where $I_{REO} = (1 - \alpha_N \alpha_I) I_{EO}$ = Reverse saturation emitter current

Similarly,

$$I_C = \alpha_N I_E - I_{RCO} (e^{V_{CB}/V_T} - 1)$$

where $I_{RCO} = (1 - \alpha_N \alpha_I) I_{CO}$

as in active mode $|V_{CB}| >> V_T$

$$\therefore I_C = \alpha_N I_E + I_{CO}$$

Standard current eq^n of transistor in active configuration

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MODELING OF BJT AS AMPLIFIER AT LOW FREQUENCIES

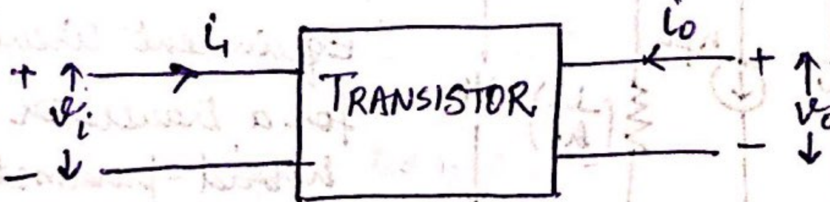
There are three small signal models for BJT used in the analysis and design of transistor amplifiers:-

(i) h-parameter model
(ii) re-model
(iii) hybrid-π model.

* h-parameter model is preferred over the other transistor models due to its advantages as under:-

(i) At low audio freq. the h-parameters are real numbers because all internal capacitances can be neglected.
(ii) If h-parameters for one configuration is known, it can be obtained for other configuration easily by a simple conversion.
(iii) h-parameters can be measured easily from the transistor dc char.
(iv) h-parameters model is independent of types of the transistor (NPN or PNP)

Hybrid (h-parameters) Model for Transistor at Low frequencies



In hybrid parameter representation, the input current and output voltage are taken as independent

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variables whereas input voltage and output current as dependent variables

$v_i = f_1(i_i, V_0)$ and

$i_0 = f_2(i_i, v_0)$

$$\begin{bmatrix} v_i \\ i_0 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ V_0 \end{bmatrix}$$

The n/w eq^n's are :-

$v_i = h_i i_1 + h_r v_0$

$i_0 = h_f i_1 + h_o v_0$

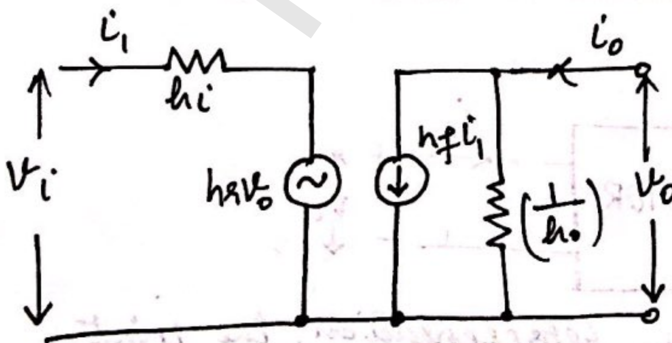
The h-parameters can be defined as :-

(i) $h_i = h_{11} = \left(\frac{v_i}{i_1}\right)_{v_0=0}$ (ohms); output short-circuited (input impedeance)

(ii) $h_r = h_{12} = \left(\frac{v_i}{v_0}\right)_{i_1=0}$; input open circuited (reverse voltage gain)

(iii) $h_f = h_{21} = \left(\frac{i_0}{i_1}\right)_{v_0=0}$; output short-circuited (forward current gain)

(iv) $h_o = h_{22} = \left(\frac{i_0}{v_0}\right)_{i_1=0}$; input open-circuited (output admittance)



Equivalent circuit for a transistor in hybrid-parameter representation

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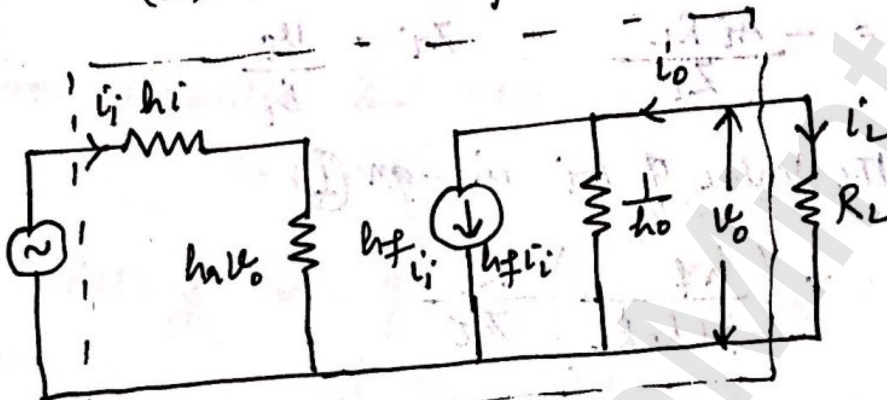
Analysis of a transistor Amplifier circuit using hybrid h-parameters

(a) Basic amplifier circuit.



(b) Hybrid Model for amplifier circuit.

A transistor amplifier consists of a transistor, load resistor, bias supply and i/p alternating signal. Its two port n/w is shown in fig. 1 and its equivalent hybrid model is shown in fig. 2

$$v_i = h_i i_1 + h_r v_o$$

$$i_o = h_f i_1 + h_o v_o$$

(i) Current gain (Ai)

$$A_i = \frac{i_L}{i_i} = \frac{-i_o}{i_i}$$

$$i_o = h_f i_1 - h_o i_o R_L$$

$$\frac{i_o}{i_i} = \frac{h_f}{1 + h_o R_L} \quad \text{—— (a)}$$

$$\therefore A_i = \frac{-h_f}{1 + h_o R_L} \quad \text{—— (1)}$$

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(ii) Voltage gain (A_v) :-

$$A_v = \frac{v_o}{v_i}$$

$$A_v = \frac{-i_o R_L}{v_i} \quad (\because v_o = -i_o R_L)$$

$$= \frac{-A_i i_1 R_L}{v_i} \quad \because i_o = i_1 A_i$$

$$A_v = -\frac{A_i R_L}{Z_i} \qquad Z_i = \frac{v_i}{i_1}$$

Subsituting the value of A_i in eqn (1)

$$A_v = -\left(\frac{h_f}{1+h_o R_L}\right)\frac{R_L}{Z_i}$$

$$A_v = \frac{-h_f}{Z_i\left(\frac{1}{R_L}+h_o\right)} \quad \text{——— (2)}$$

(iii) Input Impedeance :- (Z_i) :-

$$Z_i = \frac{v_i}{i_1}$$

$$Z_i = \frac{h_i i_1 + h_r v_o}{i_1}$$

$$Z_i = h_i - \frac{h_r i_o R_L}{i_1} \quad (\because v_o = -i_o R_L)$$

$$Z_i = h_i - h_r A_i R_L$$

Putting A_i from eqn (1)

$$Z_i = h_i - \frac{h_r h_f}{h_o + \frac{1}{R_L}} \quad \text{——— (3)}$$

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(IV) Output Impedeance :- (Z_o) :- ($R_L \longrightarrow \infty$ and $v_i \longrightarrow 0$)

$$Z_o = \frac{v_o}{i_o}$$

When $v_i = 0$, i_i can be obtained from 1st n/w eqn. as :-

$$0 = i_i h_i + h_r v_o$$

$$i_i = \frac{-h_r v_o}{h_i} \quad \text{———— (b)}$$

now consider 2nd n/w eqn :-

$$i_o = h_f i_i + h_o v_o \quad \text{———— (c)}$$

Putting value of i_i from (b) in (c) :-

$$\frac{i_o}{v_o} = h_o - \frac{h_f h_r}{h_i}$$

$$Z_o = \frac{1}{h_o - \frac{h_r h_f}{h_i}}$$

If h_r is very small and h_i is large

$$Z_o \approx \frac{1}{h_o}$$

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h-parameters Analysis of a Common-Emitter Amplifier

Let us consider a CE amplifier Circuit as shown in fig 1. The h-model for CE configuration is shown in fig-2

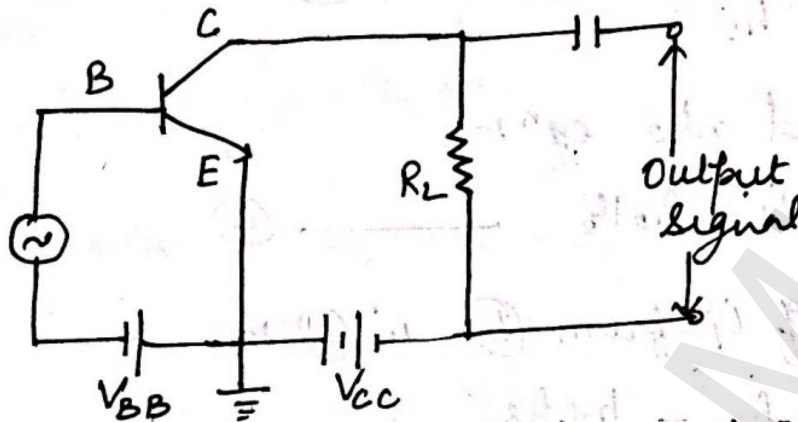

fig 1: CE PNP transistor amplifier

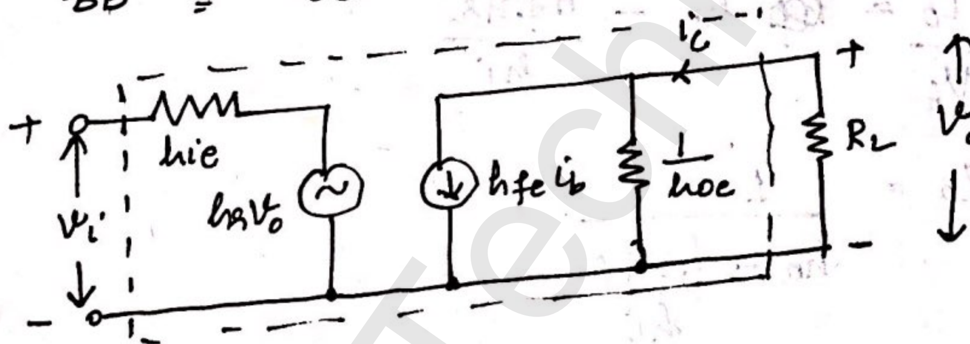

fig 2.1 Equivalent Model for CE Amplifier

In circuit of fig.2, capacitance C is neglected because impedance is assumed to be zero over the given range of freq. h_{re} is also neglected because most of the transistors give very small value ($\sim 10^{-5}$)

h_{oe} is neglected as it is of the order of 10^{-5} mho. Hence it has very large value of $\frac{1}{h_{oe}}$.

The equivalent circuit thus obtained is shown in fig.3.

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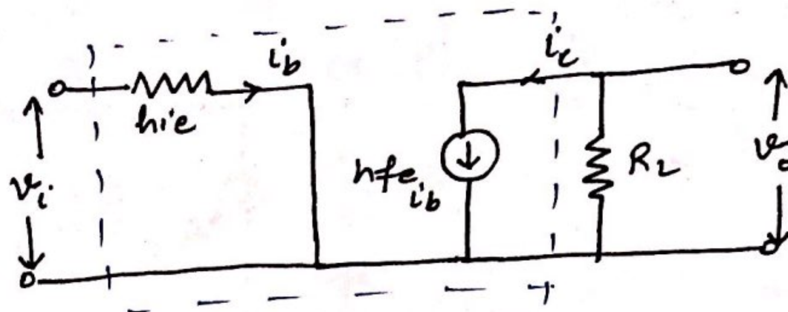

From circuit,

$$v_i = h_{ie}\, i_b$$

$$i_c = h_{fe}\, i_b$$

$$\Rightarrow h_{fe} = \frac{i_c}{i_b}$$

(i) current gain $A_{ie} = h_{fe} = \frac{i_c}{i_b}$

(ii) voltage gain $A_{ve} = \frac{v_o}{v_i}$

$$= \frac{-i_c R_L}{h_{ie}\, i_b} = \frac{-h_{fe}\, i_b R_L}{h_{ie}\, i_b}$$

$$= \frac{-h_{fe}}{h_{ie}} R_L$$

(iii) Power gain, A_{pe} = | current gain | × | voltage gain |

$$= \frac{h_{fe}^2}{h_{ie}} \times R_L$$

Hybrid Model for Common-Base Amplifier

$$v_e = h_{ib}\, i_e + h_{rb}\, v_c$$

$$i_c = h_{fb}\, i_e + h_{ob}\, v_c$$

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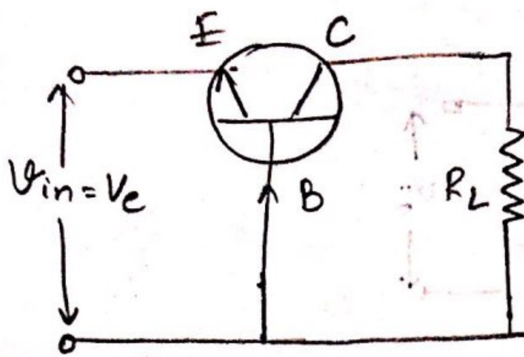
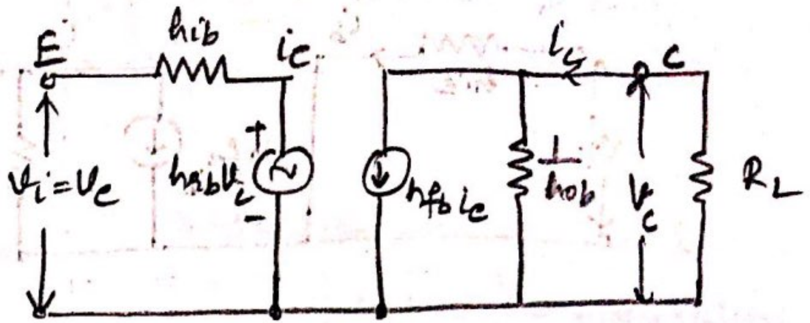


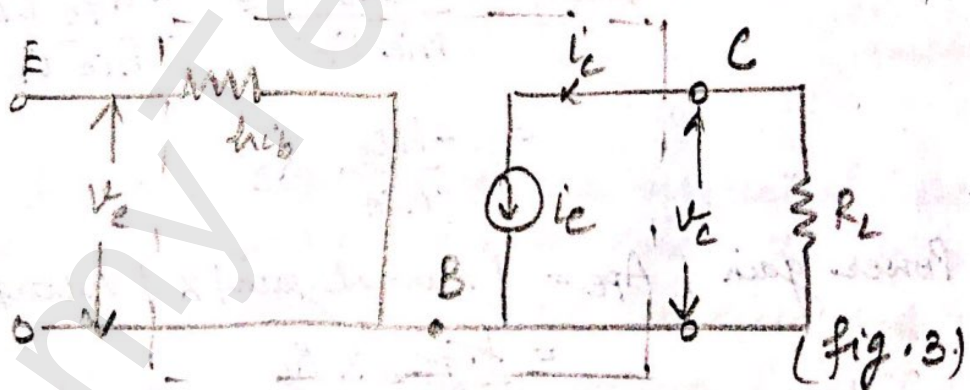
Common-base Amplifier (fig.1)



Hybrid Equivalent circuit. (fig.2)

for most of the transistors, $h_{rb} \simeq 10^{-4}$ (very small) and $\frac{1}{h_{ob}} \approx 100\,k\Omega$, hence $h_{rb}\,V_c$ (voltage generator) and shunt impedance $\frac{1}{h_{ob}}$ can be omitted. Thus simplified circuit is shown in fig3, with reduced n/w eq^{n}s

$$\left.\begin{aligned} V_e &= h_{ib}\,i_e \\ i_c &= h_{fb}\,i_e \end{aligned}\right\}$$



(fig.3)

1.) Current gain $A_i = \frac{i_c}{i_e}$

$$\boxed{A_i = h_{fb}}$$

2.) Voltage gain $A_v = \frac{V_c}{V_e} = \frac{-i_c R_L}{V_e}$ $(\because V_c = V_o = -i_c R_L)$

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$$A_v = \frac{-i_e h_{fb} R_L}{h_{ib} i_e}$$

$$A_v = -\frac{h_{fb}}{h_{ib}} R_L$$

where $\frac{h_{fb}}{h_{ib}} = g_m =$ transconductance

$$\boxed{A_v = -g_m R_L}$$

(iii) <u>Power gain :-</u>

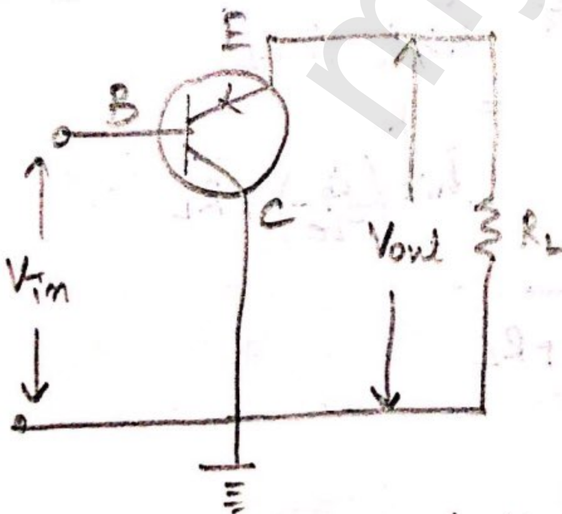
$$A_p = |A_i||A_v| = \frac{h^2_{fb} R_L}{h_{ib}}$$

In common-base configuration $A_i \leq 1$,

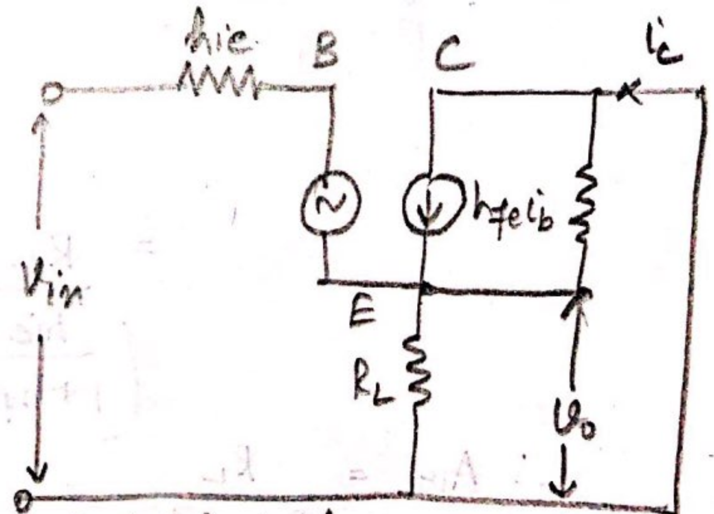
$$A_p \approx |A_v| = \frac{h_{fb}}{h_{ib}} R_L$$

$$\boxed{A_p = g_m R_L}$$

Hybrid Model for Common Collector Amplifier



Common Collector Amplifier



hybrid equivalent ckt.

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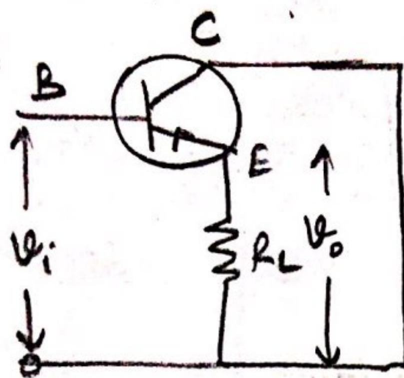

Redrawn CC circuit

Fig 3.

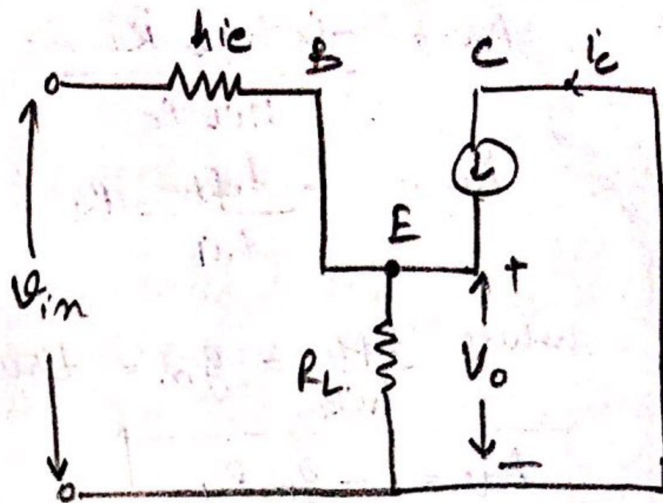

fig.4.

Hybrid equivalent circuit, can be simplified by ignoring $h_{re} v_c$ and $\frac{1}{h_{oe}}$. Thus simplified is shown in fig 4.

from circuit,

$$i_e = -(i_c + i_b) = -(1+h_{fe}) i_b$$

$$v_i = h_{ie} i_b + (-i_e) R_L \quad (\because i_c = h_{fe} i_b)$$

$$v_o = -i_e R_L$$

(i) Current gain (A_{ic}) :- $A_{ic} = \frac{i_e}{i_b} = -(1+h_{fe}) \approx -h_{fe}$

(ii) Voltage gain (A_{vc}) :- $A_{vc} = \frac{v_o}{v_i} = \frac{-i_e R_L}{h_{ie} i_b - i_e R_L}$

$$= \frac{R_L}{h_{ie}\left(\frac{i_b}{-i_e}\right) + R_L}$$

$$= \frac{R_L}{\left(\frac{h_{ie}}{1+h_{fe}}\right) + R_L}$$

$$\therefore A_{vc} = \frac{R_L}{R_L + \left(\frac{h_{ie}}{h_{fe}}\right)}$$

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Since $\frac{h_{fe}}{h_{ie}} = g_m =$ trans conductance

$$A_{vc} = \frac{g_m R_L}{g_m R_L + 1} \leq 1$$

(iii) <u>Power gain</u>

$$A_{pc} = |A_{vc}||A_{ic}| = \frac{h_{fe} g_m R_L}{g_m R_L + 1}$$

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FIELD EFFECT TRANSISTORS

A field effect transistor is a unipolar device in which current conduction is only by one polarity carrier (i.e. majority carrier). Flow of current is controlled by electric field.

FET can be categorized into two types:-

(i) Junction field effect transistor (JFET)
(ii) Metal oxide semiconductor field effect Transistor (MOSFET).

* FET has many advantages over BJT:-
  (i) In BJT output current is controlled by input current, so names as current controlled device, while FET is voltage controlled device.
  (ii) The input to BJT amplifier involves a F.B. PN-junc^n with low resistance, while input to FET involves a reverse biased PN-junc^n with very high resistance.
  (iii) Thermally stable than BJT
  (iv) Less noise than BJT.

* The main drawback of FET is relatively small gain B.W. product

JUNCTION FIELD EFFECT TRANSISTOR (JFET)

It can be of two kinds

(i) N-channel. It is made of N-type semiconductor
(ii) P-channel. It is made of P-type semiconductor

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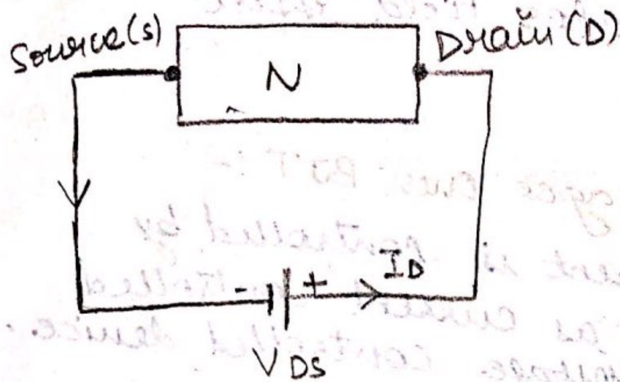
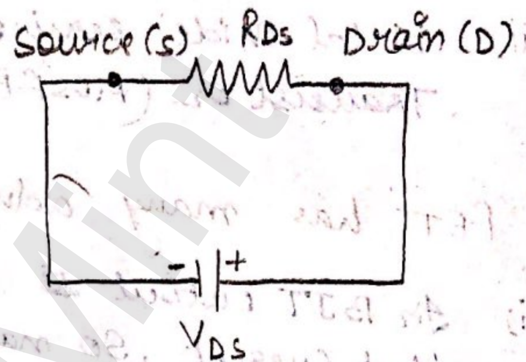
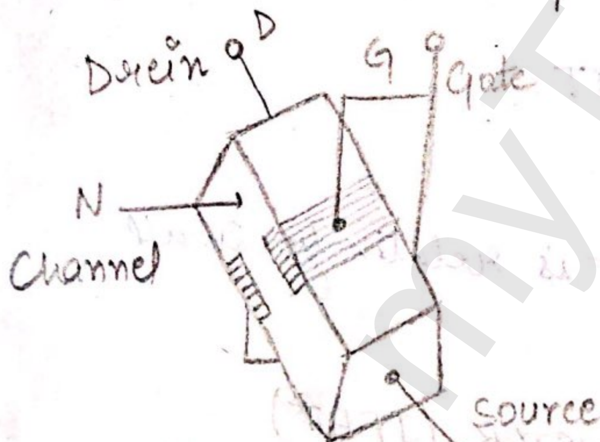
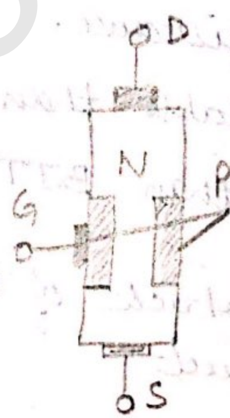
* A JFET is a three terminal device namely, source drain and gate terminal. It consists of a P-type or n-type silicon bar containing two P-N junctions as shown in fig. The two p-n junction forming diodes are connected internally and a common terminal called gate is taken out

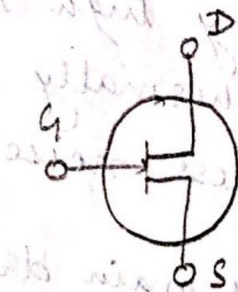




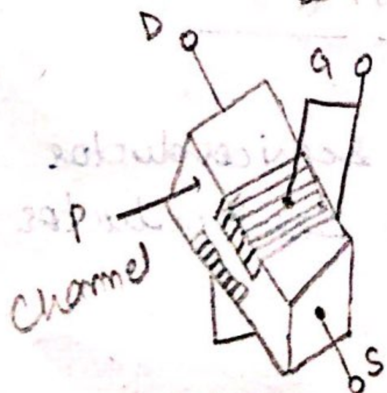
Symbol of JFET | CONSTRUCTION

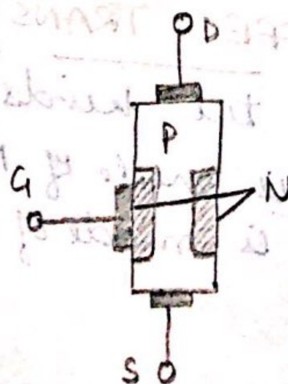


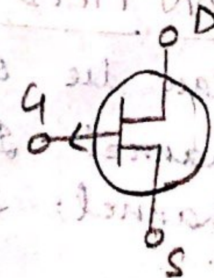




Nchannel JFET







P-Channel JFET

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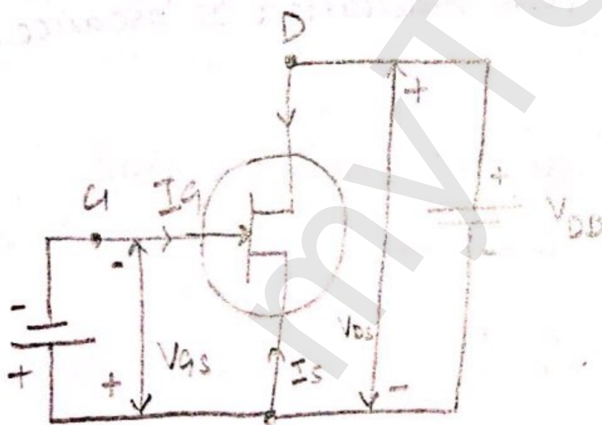
1) **Source :-** Terminal through which majority carriers enter the bar.

2) **Drain :-** Terminal through which majority carriers leave the bar

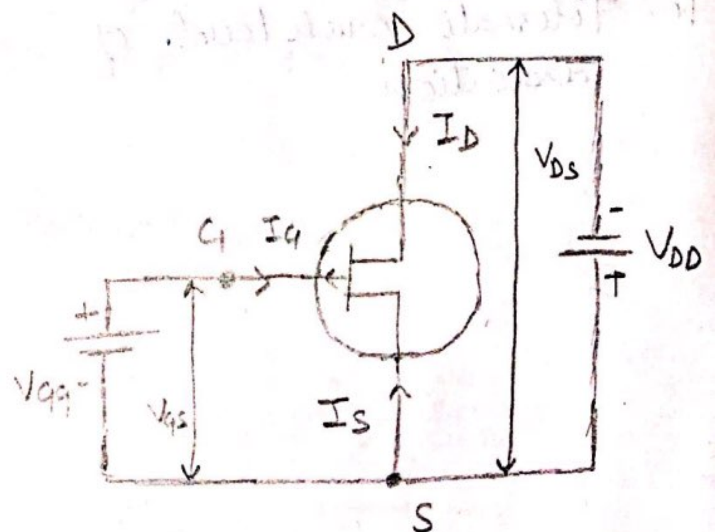
3) **Gate :-** form P-N junc^n's

4) **Channel :-** Space b/w two gates through which majority carriers pass.

CIRCUIT SYMBOL & NOTATION



N-Channel



P- Channel

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JFET	BJT
1. Unipolar device	Bipolar device
2. Voltage controlled device	Current controlled device
3. Low noise level	High noise level
4. High input impedeance	Low input impedeance
5. Gain is characterstised by transconductance	Gain is characterstised by Voltage gain / Current gain.
6. Better thermal stability.	less thermal stability
7. High power gain	Low power gain
8. Fabrication of FET is simple.	Fabrication is little tough
9. Smaller size, longer life, high efficiency	less life & less efficiency in comparision to JFET
10. Tolereate much level of radiation	Less radiation tolereance.

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WORKING

* Suppose that gate g has been R.B. and drain battery V_{DD} is not connected. Depletion layer formed symmetrically about the gate (as in fig.1).
* Further consider drain battery connected & gate battery removed. Suppose R_{DS} is resistance from drain to source. So, due to current I_D there will be uniform voltage drop from drain to source. Consider potential at two points A and B. ($V_A > V_B$) (as shown in fig.2)
* Now in proper working of JFET. Both batteries V_{GG} & V_{DD} connected simultaneously. Reverse biasing effect on P-N juncn is stronger near drain than near source. Due to this reason penetration at A is more than B.

When gate-bias is increased further, a stage is reached when two depletion region touch each other & I_D becomes zero.

NOTE :- Since -ve gate voltage control current so, it is called voltage controlled device.

fig.1

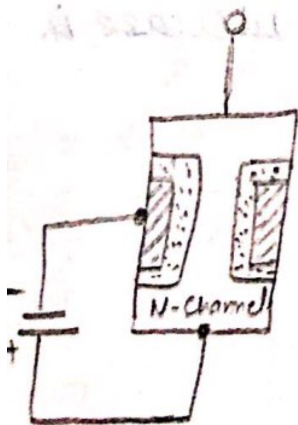


fig.2

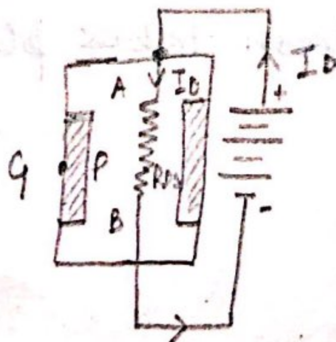
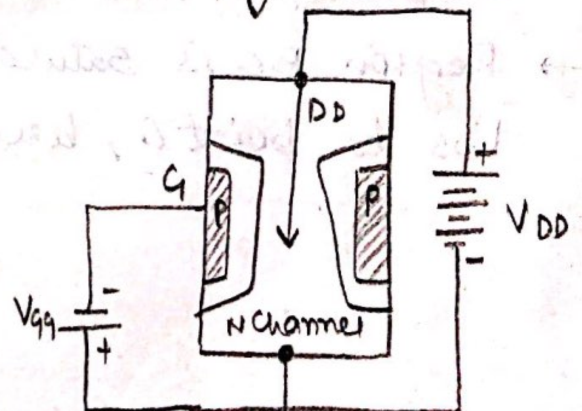
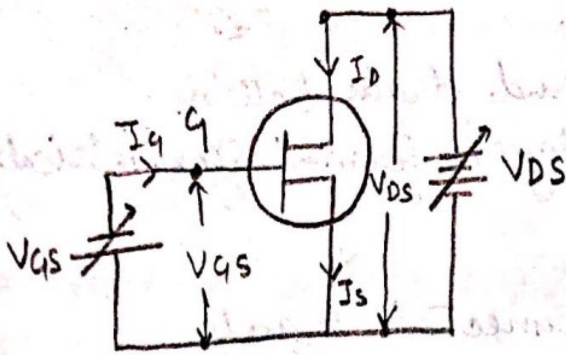


fig.3



JFET CHARACTERSTICS



* Types of static characteristics :-

1.) Static drain characteristics. (I_D Vs V_{DS})

→ $V_{GS} = 0$ (Gate is shorted to source)

→ $V_{DS} = 0$, hence $I_D = 0$.

→ As $V_{DS} \uparrow$, $I_D \uparrow$ linearly upto A (knee point)

→ Increasing I_D, reverse bias the gate junc^n and channel begins to constrict.

→ As V_{DS} increases, I_D reaches to point B. (pinch-off point)

→ At pinch off point channel is more or less blocked

→ Pinch-off is defined as the min. drain to source voltage where the drain current approaches a constant value. Pinch-off doesnot mean I_D cut off or channel is completely closed & hence I_D doesnot reduce to zero

→ Region BC is saturation, with continuous increase in V_{DS} to point C, breakdown takes place.

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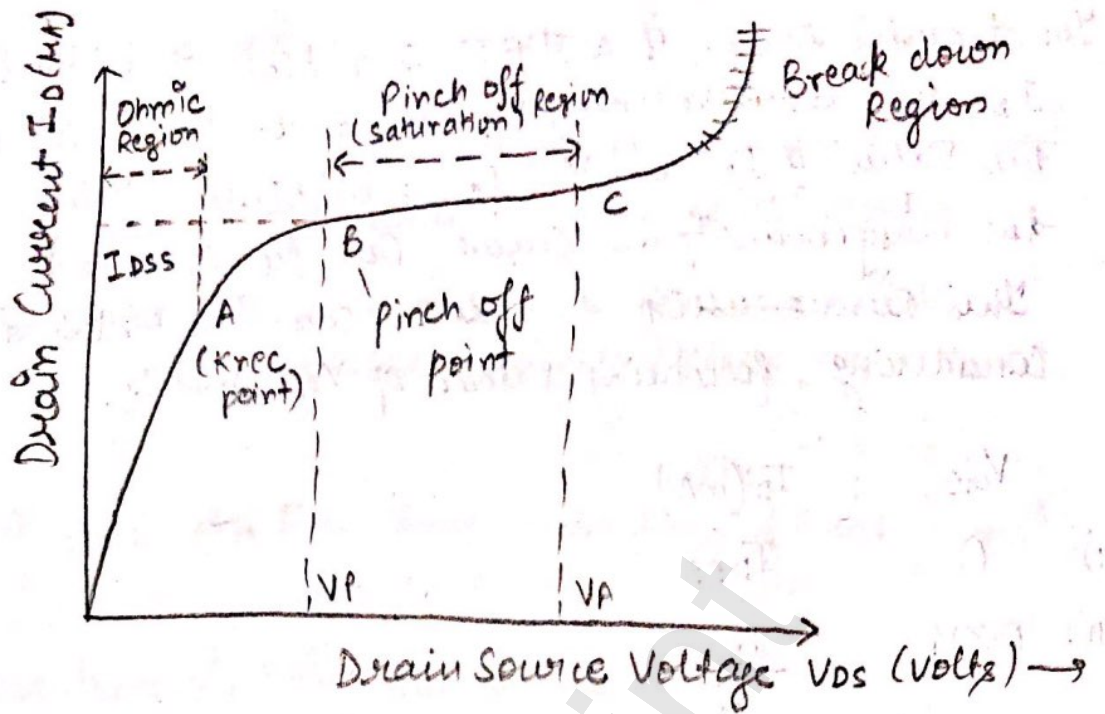

TRANSFER CHARACTERSTICS (OR TRANS CONDUCTANCE CHARACTERSTICS)

I_D (mA)

I_D (mA)

IDSS

$V_{GS} = 0V$

$V_{GS} = -1V$

$V_{GS} = -2V$

$V_{GS} = -3V$

V_{GS} (V)

-4 -3 -2 -1 0

0 5 10 15 20 25 VDS

↑

$I_D = 0mA$, $V_{GS} = V_P = V_{GS(off)}$

$V_{GS} = -4V = V_P$

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The transfer char. of a JFET is a plot of output current I_D vs input voltage, V_{GS} for a constant. By reading the value of I_D and V_{GS} for a particular value of V_{DS} the transconductance curve can be drawn.
This curve using 4 points can be obtained by considering following values of V_{GS} and I_D.

	V_{GS}	I_D (mA)
(i)	0	I_{DSS}
(ii)	$0.3V_p$	$\frac{I_{DSS}}{2}$
(iii)	$0.5V_p$	$\frac{I_{DSS}}{4}$
(iv)	V_p	0

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where I_D = drain current
I_{DSS} = Value of saturation drain current at $V_{GS} = 0V$
V_{GS} = gate to source voltage
V_P = V_{GS} at $I_{DS} = 0$ (pinch-off voltage)

JFET Parameters :-

(i) Drain Resistance :- $r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}}$; where V_{GS} is constant.

(ii) Transconducance (g_m) :- $\left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$, where V_{DS} is constant.

(iii) Amplification factor (μ) = $-\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D}$; where I_D is constant

-ve sign indicates that when V_{GS} is increased, V_{DS} is decreased for a constant I_D.

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JFET Applications :-

(i) JFET are used in cascade amplifiers in test and measuring devices, because of low level noise.

(ii) The can be used in Voltage Variable resistor (VVR) because of variable resistance in Ohmic region.

(iii) They are used in low freq. amplifiers (hearing aid etc.), because of low coupling capacitor

(iv) They can be used in analog switches

(v) They have very high power gain.

(vi) They are preferred in computers and other Ic's because of small sizes.

METAL OXIDE SEMICONDUCTOR FET :-

In this device, gate consists of metal and kept isolated from channel by inserting a thin layer of SiO_2 insulator. For this reason they are also called IGFETs (Insulated Gate field Effect transistor)

Types :-

1. Enhancement Type
2. Depletion Type.

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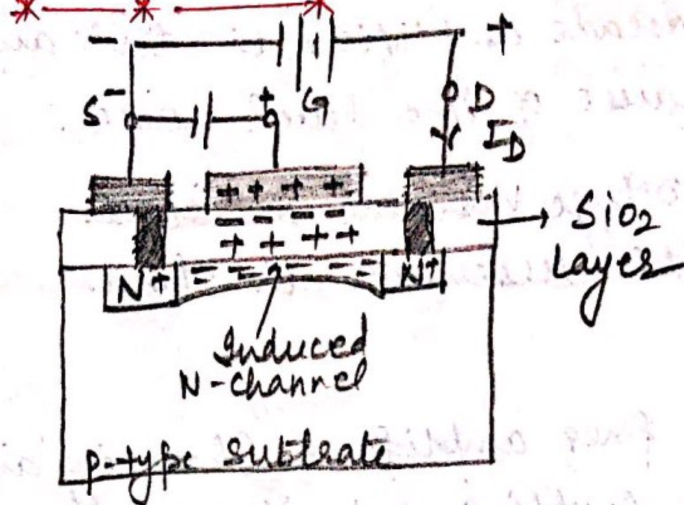
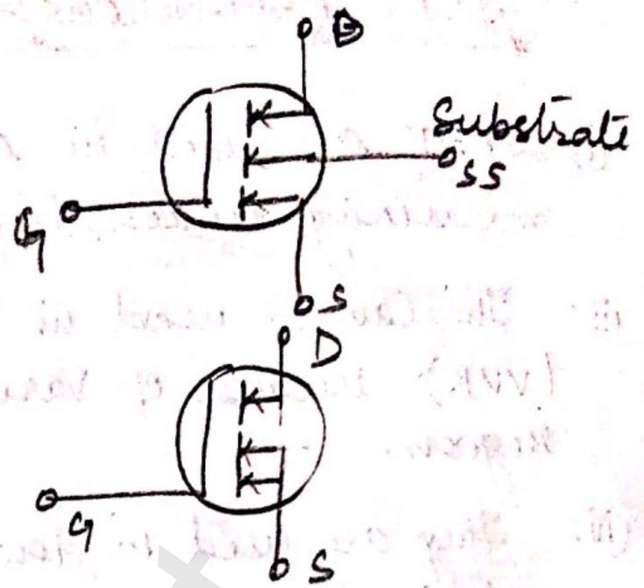
1.7 E-MOSFET





MOSFET's donot have continous channel for conduction.

Construction:- A lightly doped P-type semiconductor is taken as a substrate and two lightly doped N+ type regions diffused in it. One N- region is source and other is drain D. These are seprated by distance 1mm. A thin layer of insulating material i.e. (SiO_2) is then deposited leaving only two holes for connections to the source and the drain. A thin layer of a metal is now deposited over the SiO_2 This mettalic layer acts as gate, insulator (SiO_2) and semiconductor channel together forms a ||el plate capacitor which replace the P-N junc^n of JFET. Input Impedeance is very high due to insulating layer ($10^{10} - 10^{15} \Omega$).

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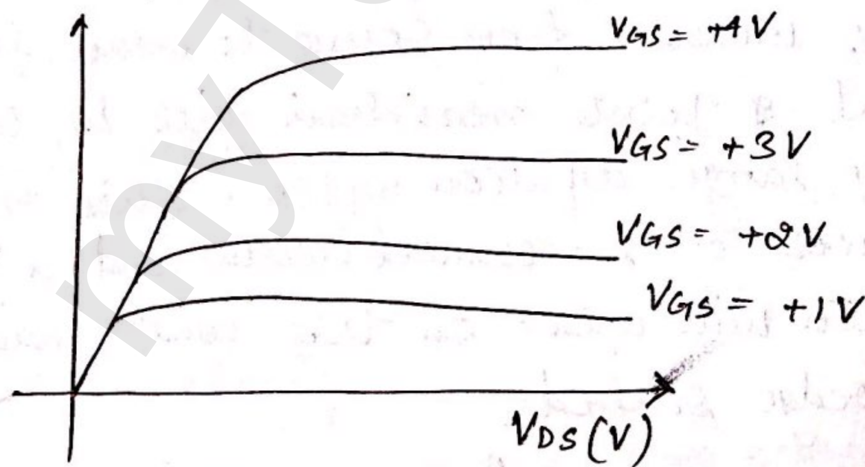
OPERATION

Suppose $V_{GS} = 0$, a very small drain current will flow due to minority carriers present in the substrate of p-type. When +ve voltage is applied at the gate w.r.t. source i.e. V_{GS} is +ve, an electric field is produced through capacitor that draws minority carriers from the substrate towards the n-region b/w source and drain forming channel of N-type material i.e. +ve potential at the gate induces opp. charges between sources and drain which acts as N-channel. Hence this channel is known as induced channel. As a result conductivity increases and current flows through this channel. Therefore drain current strongly increases with increase in V_{GS}.

Drain char. of N-channel EMOSFET



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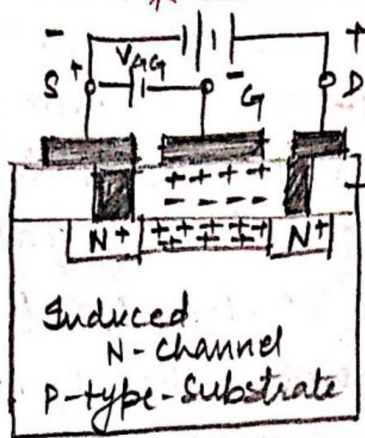
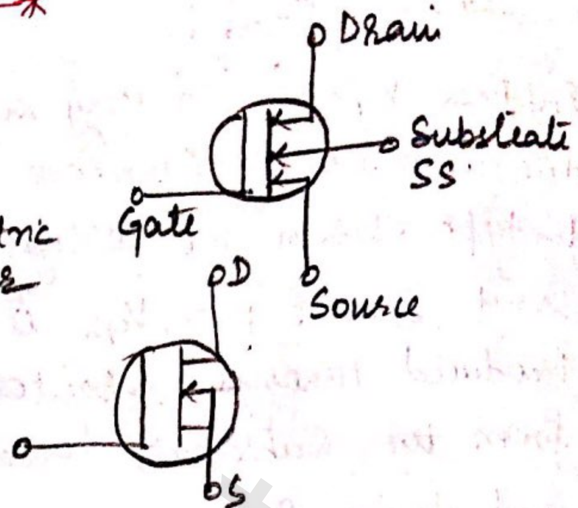
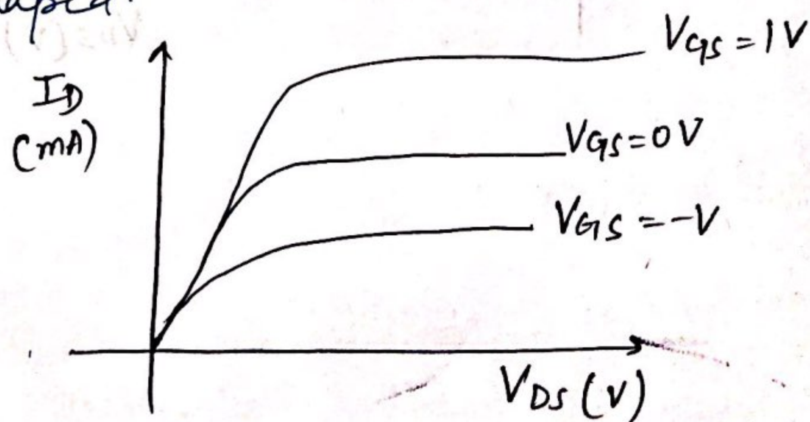
DEPLETION TYPE MOSFET





When $V_{GS} = 0$, a very small drain current flows due to minority carriers in p-type substrate. When -ve voltage is applied at the gate w.r.t. source V_{GS} becomes +ve, thus an electric field is produced which is perpendicular to the capacitor. In this process free carriers present in the substrate are moved away from insulator-channel boundary. This create depletion layer at channel. Width of depletion layer at gradually increases from source to drain because potential of points near drain will be larger creating larger depletion width. This results in narrower of the channel width and a pinch off situation will arise. In this condⁿ channel will be wedge shaped.



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BOOLEAN ALGEBRA AND MINIMIZATION TECHNIQUES

BOOLEAN POSTULATES

1. COMMUTATIVE LAW :-
   (a.) $a + b = b + a$
   (b.) $a \cdot b = b \cdot a$

2. ASSOCIATIVE LAW :
   (a.) $a + (b + c) = (a + b) + c$
   (b.) $a \cdot (b \cdot c) = (a \cdot b) \cdot c$

3. Distributive Law :-
   (a.) $a + (b \cdot c) = (a + b) \cdot (a + c)$
   (b.) $a \cdot (b + c) = (a \cdot b) + (a \cdot c)$

4. Identity elements
   (i) $a + 0 = 0 + a = a$
   (ii) $a \cdot 1 = 1 \cdot a = a$

5. Complement Law :-
   (i) $a + \overline{a} = 1$
   (ii) $a \cdot \overline{a} = 0$

PRINCIPLE OF DUALITY

In boolean algebra if the dual of any expression is desired simply replace every '+' with '.' and every '.' with '+' or every '0' with '1' and every '1' with '0'

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S.No.	Boolean Expression	Dual Expression
1.	$A+0=A$	$A\cdot 1=A$
2	$A+1=1$	$A\cdot 0=0$
3.	$A+A=A$	$A\cdot A=A$
4.	$A+\overline{A}=1$	$A\cdot\overline{A}=0$

BOOLEAN THEOREM

1. **TAUTOLOGY LAW:-**

(i) $a+a=a$

(ii) $a\cdot a=a$

Proof:- (i) $L.H.S=(a+a)$

$=(a+a)\cdot 1$

$=(a+a)(a+\overline{a})$

$=a+a\cdot\overline{a}$

$=a=R.H.S$

(ii) $L.H.S=a\cdot a$

$=a\cdot a+0$

$=a\cdot a+a\cdot\overline{a}$

$=a(a+\overline{a})$

$=a=R.H.S$

2. UNION LAW :-

(i) $a + 1 = 1$

(ii) $a + 0 = a$

Proof :- (i) $L.H.S = a + 1$

$= (a+1) \cdot 1$

$= (a+1) \cdot (a+\bar{a})$

$= a + 1 \cdot \bar{a}$

$= a + \bar{a} = 1 = R.H.S$

(ii) $L.H.S = a + 0$

$= a + (a \cdot \bar{a})$

$= (a+a) \cdot (a \cdot \bar{a})$

$= a \cdot 1$

$= a = R.H.S.$

3. INTERSECTION LAWS :-

(i) $a \cdot 1 = a$

(ii) $a \cdot 0 = 0$

(i) $L.H.S = a \cdot 1$

$= a \cdot (a + \bar{a})$

$= a \cdot a + a \cdot \bar{a}$

$= a + 0 = a = R.HS.$

(ii) $L.H.S = a \cdot 0$

$= a \cdot 0 + 0$

$= a \cdot 0 + a \cdot \bar{a}$

$= a(0 + \bar{a})$

$= a \cdot \bar{a} = 0 = R.H.S$

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4. ABSORPTION LAWS:-

(i) $a \cdot (a+b) = a$

(ii) $a + ab = a$

(iii) $a + \bar{a}b = a + b$

(iv) $a \cdot (\bar{a} + b) = a \cdot b$

Proof:- (i) $a \cdot (a+b)$

$= a \cdot a + a \cdot b$

$= a + ab$

$= a \cdot 1 + ab$

$= a(1+b)$

$= a = R \cdot H \cdot S$

(ii) $a + ab = a \cdot 1 + ab$

$= a(1+b)$

$= a = R \cdot H \cdot S.$

(iii) $L \cdot H \cdot S = a + \bar{a}b$

$= (a+\bar{a})(a+b)$ (Using distributive law)

$= 1 \cdot (a+b)$

$= a+b$

(iv) $L \cdot H \cdot S = a \cdot (\bar{a}+b)$

$= a \cdot \bar{a} + a \cdot b$

$= 0 + ab$

$= ab = R \cdot H \cdot S.$

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5. DOUBLE NEGATION LAW

$$\overline{\overline{a}} = a$$

L.H.S $= \overline{\overline{a}}$

$= \overline{\overline{a}} \cdot 1$

$= \overline{\overline{a}} \cdot (a + \overline{a})$

$= (\overline{\overline{a}} \cdot a) + (\overline{\overline{a}} \cdot \overline{a})$

$= \overline{\overline{a}} \cdot a + 0$

$= \overline{\overline{a}} \cdot a + \overline{a} \cdot a$

$= (\overline{\overline{a}} + \overline{a}) \cdot a$

$= 1 \cdot a$

$= a =$ R.H.S

6. DE-MORGAN'S LAW

(i) $\overline{a+b} = \overline{a} \cdot \overline{b}$ V. imp.

(ii) $\overline{a \cdot b} = \overline{a} + \overline{b}$

Proof:- (i) $\overline{a+b} = \overline{a} \cdot \overline{b}$

It is sufficient to prove that,

do the proof from book

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Ques 1. Find the dual of the following boolean expression :-

(i) $A+AB=A$

Dual expression of $A+AB = A\cdot(A+B)$

{Replace '+' with '.' and '.' with '+'}

(ii) $A+\overline{A}B = A+B$

$A\cdot(\overline{A}+B) = A\cdot B$

Ques 2. Prove the following expressions :-

(i) $A+\overline{A}B+AB = A+B$

(i) $L.H.S = A+\overline{A}B+AB$

$= A(1+B)+\overline{A}B$

$= A+\overline{A}B$

$= (A+\overline{A})(A+B)$

$= 1\cdot(A+B) = R.H.S$

(ii) $ABCD + A\overline{B}CD = ACD$

$L.H.S = ABCD + A\overline{B}CD$

$= ACD(B+\overline{B})$

$= ACD = R.H.S$

(iii) $AB+\overline{A}C+BC = AB+\overline{A}C$

$L.H.S = AB+\overline{A}C+BC$

$= AB+\overline{A}C+(A+\overline{A})BC$

$= AB+\overline{A}C+ABC+\overline{A}BC$

$= AB+ABC+\overline{A}C+\overline{A}BC$

$= AB(1+C)+\overline{A}C(1+B) = AB+\overline{A}C = R.H.S$

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(iv) $(X+\overline{Y}+XY)(X+\overline{Y})(\overline{X}Y) = 0$

$L.H.S = (X+\overline{Y}+XY)(X+\overline{Y})(\overline{X}Y)$

$= (X+\overline{Y}+XY)(X+\overline{Y}+0)(\overline{X}Y)$

$= ((X+\overline{Y})+XY.0)(\overline{X}Y) = (X+\overline{Y}).(\overline{X}Y)$

$= X\overline{X}Y + \overline{X}Y\overline{Y}$

$= 0.Y + \overline{X}.0 = 0 = R.H.S$

(v) $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\,\overline{C} = \overline{A} + \overline{B+C}$

$\overline{A}\,\overline{B}(\overline{C}+C) + \overline{A}B(\overline{C}+C) + A\overline{B}\,\overline{C}$

$\overline{A}\,\overline{B} + \overline{A}B + A\overline{B}\,\overline{C}$

$= \overline{A}(\overline{B}+B) + A\overline{B}\,\overline{C}$

$= \overline{A} + A\overline{B}\,\overline{C}$

$= \overline{A} + \overline{B}.\overline{C}$ $(\because A+\overline{A}B = A+B)$

$= \overline{A} + \overline{B+C}$ (using De-Morgan's Law)

Hence Proved.

Ques 3. Simplify :-

$Y = \overline{A.B}(A+\overline{B})$

$Y = (\overline{A}+\overline{B})(A+\overline{B})$

$= \overline{A}A + \overline{B}A + \overline{A}B + \overline{B}B$

$= 0 + A\overline{B} + \overline{A}B + 0$

$= A\overline{B} + \overline{A}B = A \oplus B$

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LOGIC GATES

Logic gates are building blocks of any digital system. They can be constructed by using simple switches, relays, diodes, Transistors or integrated circuits.
It is defined as an Electronic device with logical manipulation and one or more than one inputs and only one output is called logic gate.

* The logic gates are classified as :-

(i) Basic Gates :- AND Gate
OR Gate
NOT Gate

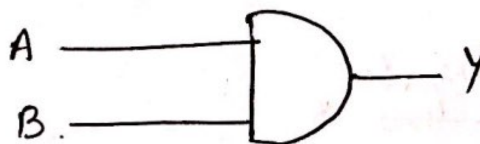
(ii) Universal Gates :- NAND gate
NOR gate

(iii) Special purpose gates :- Exclusive OR gate
Exclusive NOR gate

AND GATE

$Y = A \text{ (AND) } B = A \cdot B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



* The O/P of AND gate is '1' if and only if all the inputs are at high logic i.e. 1

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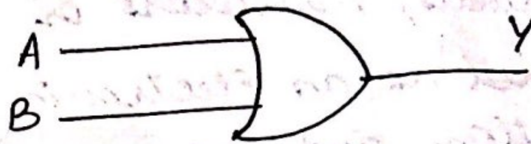
OR Gate

$Y = A \text{(OR)} B = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



* The output of an OR gate is 1 if and only if any one or more than one input at any time is high i.e. '1'

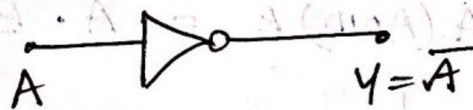
NOT Gate

It is also termed as inverter

$Y = \text{(NOT)} A = \overline{A}$

The NOT opereation is also termed as inversion or complementation

A	$Y=\overline{A}$
0	1
1	0



NAND Gate

The ~~NAD~~ NAND gate is basically NOT-AND gate. It It is also termed as universal gate since any boolean expression can be realized using it.

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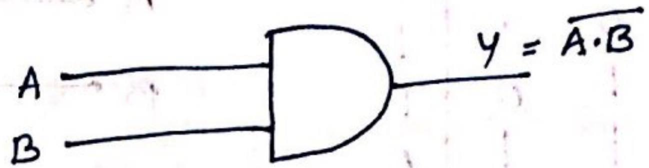
$Y = \overline{A \cdot B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



* The o/p of a NAND gate is 1 if and only if any one or more than one input at any time is low i.e. at logic '0'.

NOR Gate

The NOR gate is basically NOT-OR gate. It is also a universal gate.

$Y = \overline{A + B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

EXCLUSIVE-OR GATE

$Y = A \text{ (EX-OR) } B$

$= A \oplus B$

$Y = \overline{A}B + A\overline{B}$

* The output is 1 if and only if the inputs are different.

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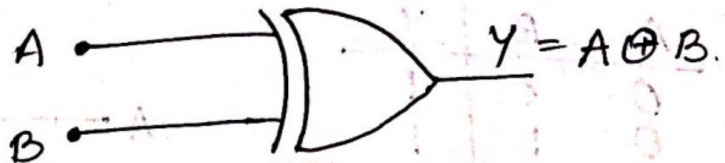
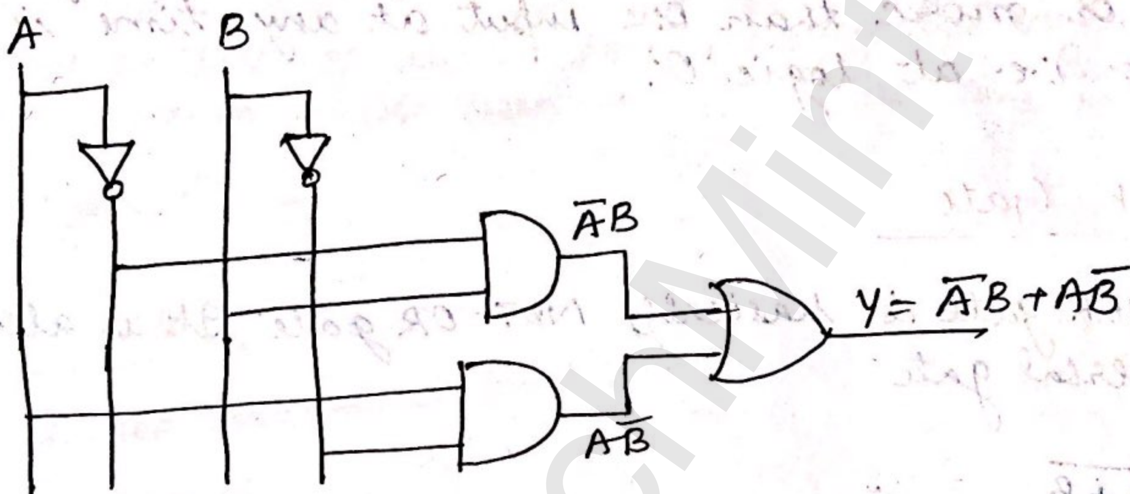
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



$Y = \bar{A}B + A\bar{B}$



EXCLUSIVE NOR gate

$Y = A\,(\text{EX-NOR})\,B$

$= A \odot B = \overline{A \oplus B}$

$= AB + \bar{A}\bar{B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

* The o/p is 1 if and only if the inputs are same.

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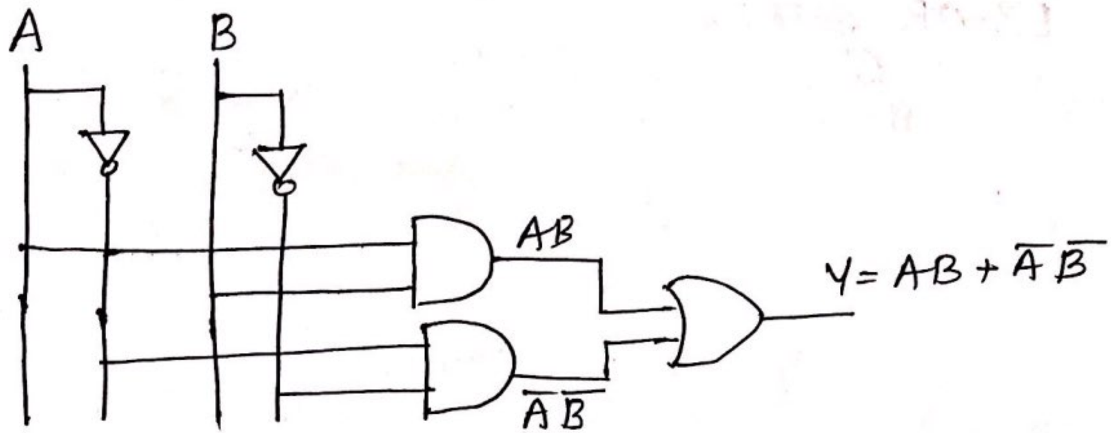
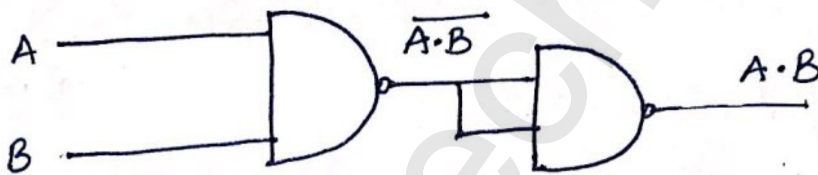
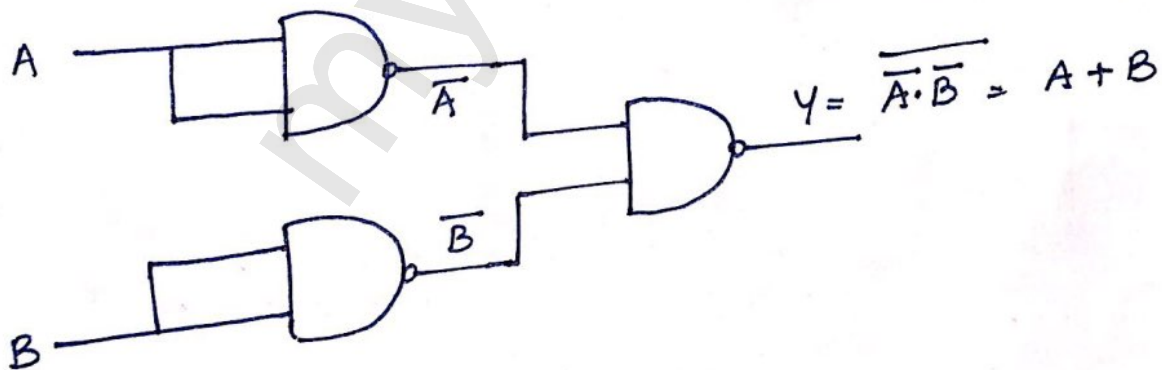


Ques. Construct the following logic gates with the help of NAND gate

(i) AND gate :-



(ii) OR gate :-



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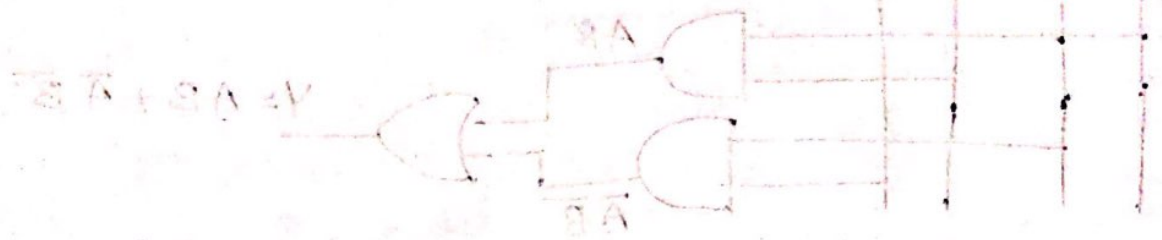
(iii) EX-OR gate:-

[illegible]



Q. Realise the logic expression $Y = \overline{BC} + \bar{A}\bar{C} + \overline{\bar{A}B}$ using basic gates.

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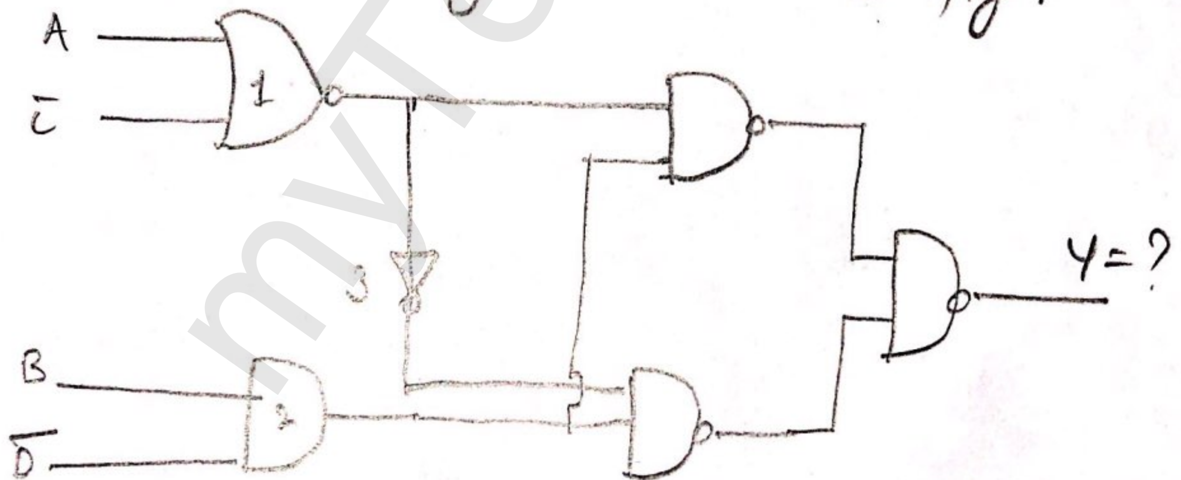
Q. Implement $Y = \overline{AB} + A + (\overline{B+C})$ using NAND gates only.

Ques. Simplify the logic ckt. shown in fig.



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